
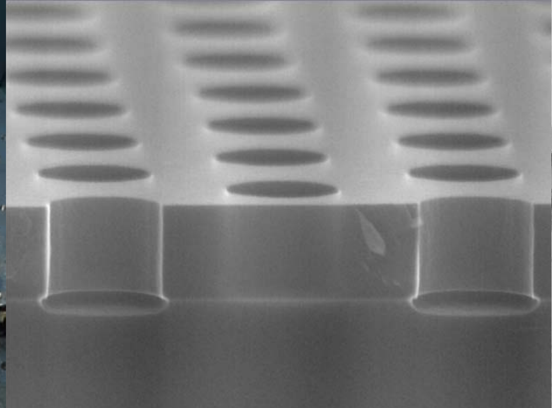
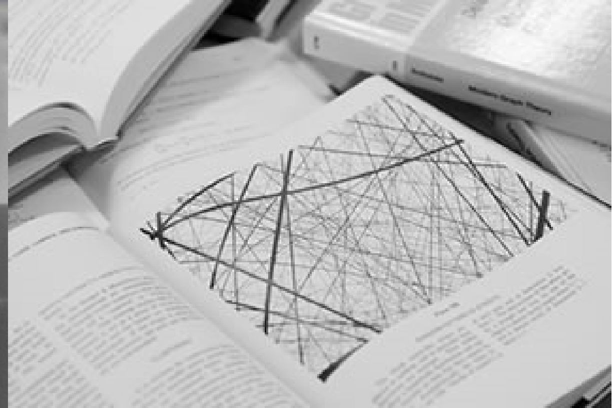

ISPEC, Tokyo, Nov. 20, 2013

Investigating the robustness of all-optical NAND gates composed by microring cavities

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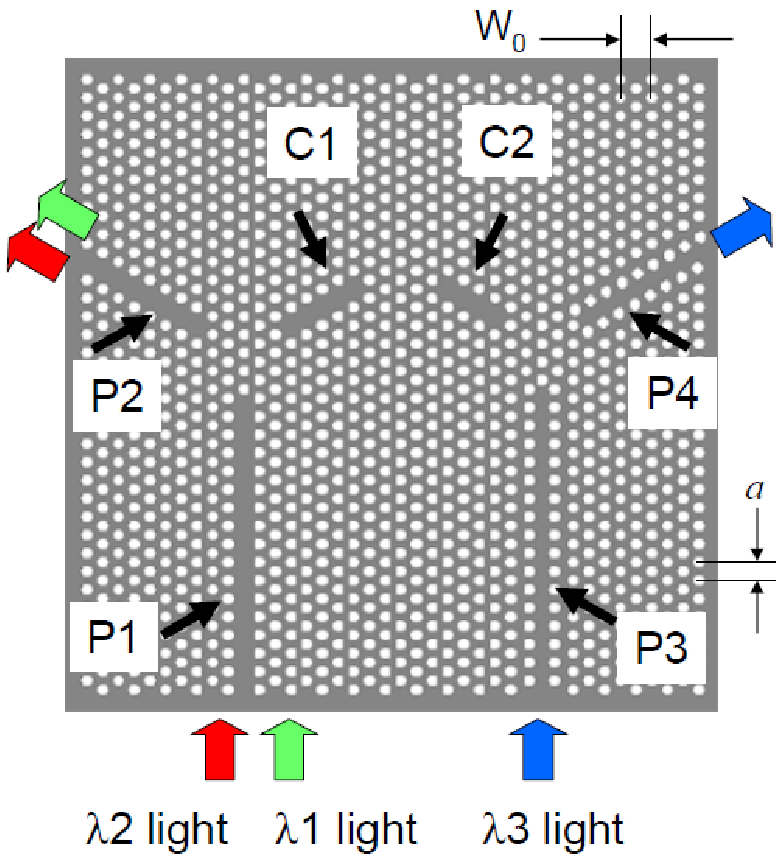
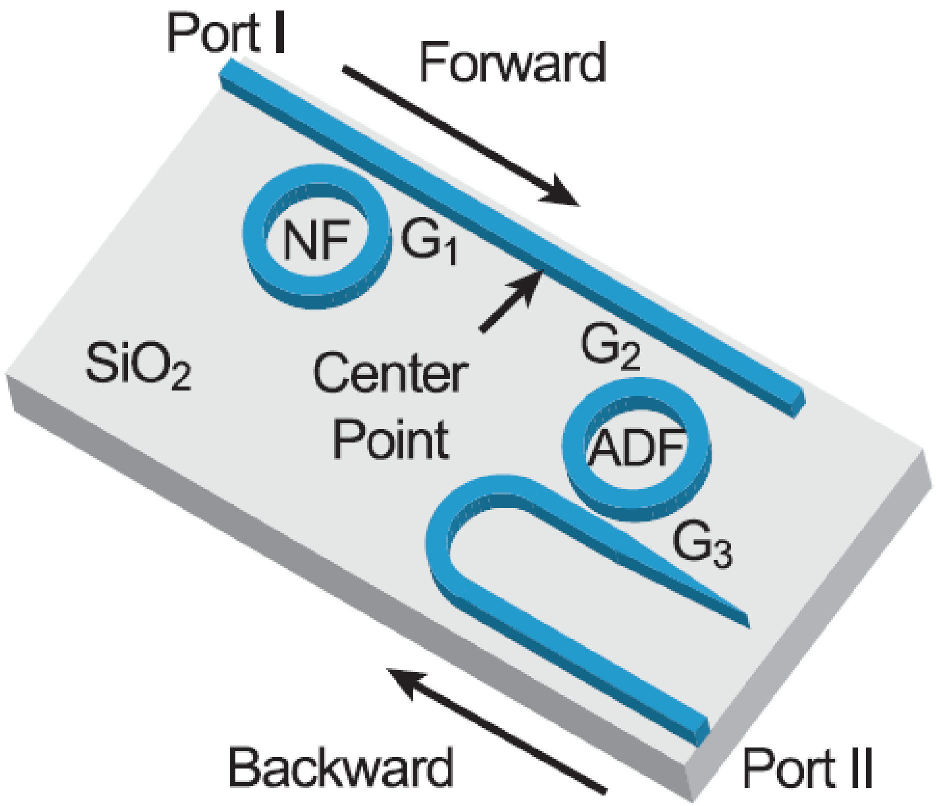
All-optical logic gates on chip

Calculation: Optical flip-flop



A. Shinya, *et al*., Opt. Express **14**, 3 (2006)

Experiment: Optical diode



Li Fan, *et al.* Science **335**, 447 (2012)

►A gap exists between numerical calculation & experiment

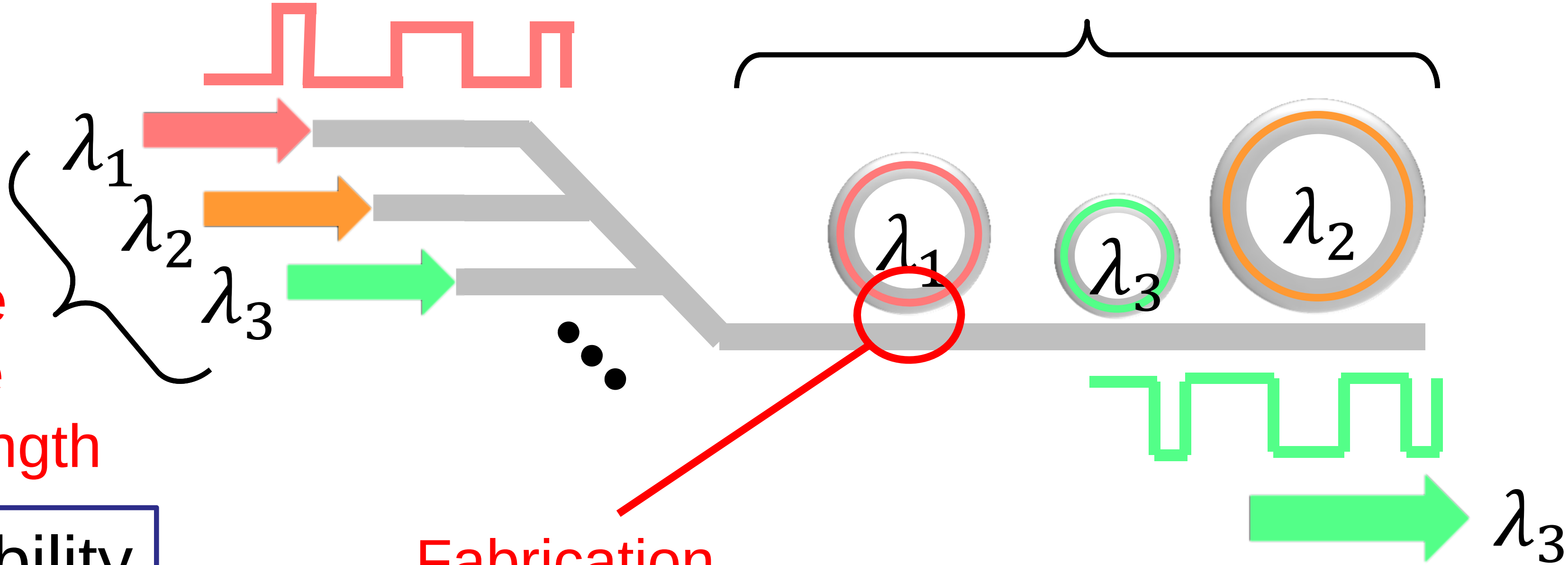
What makes experimental implementation difficult?

Small robustness

Input power fluctuations

Design complexity

Different cavity designs



Require multiple wavelength

Low scalability

Fabrication tolerance unknown

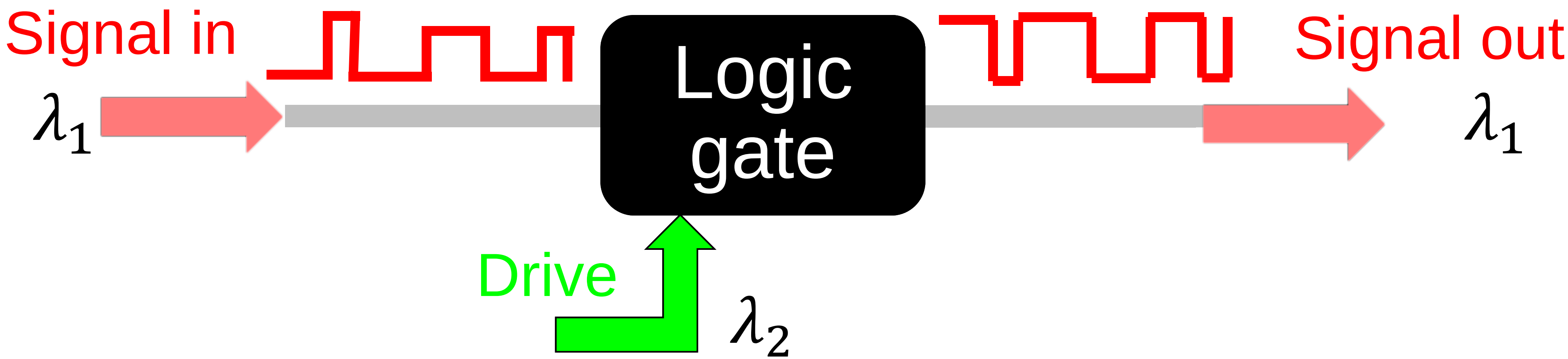
Different in/out wavelength

Low scalability

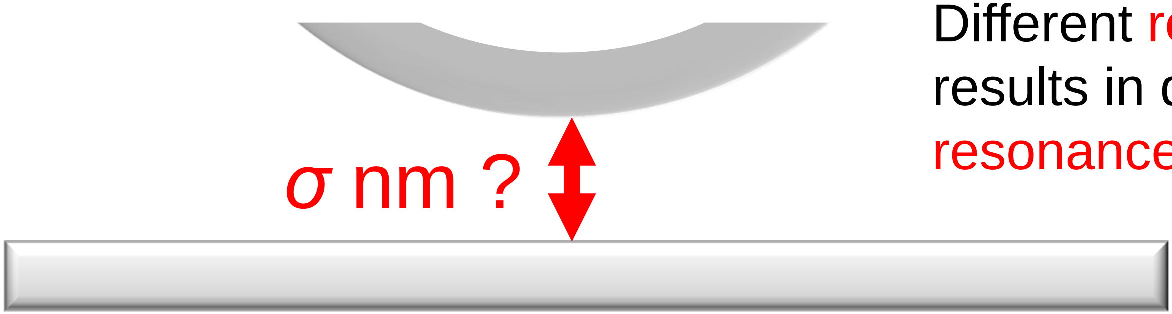
Low fabrication tolerance

Required characteristics

Simple design / high scalability



Large error tolerance (first step is to know such effect)



Different resonances / gap distances results in different resonance / coupled strength

Fabrication error vs. successful operation ?

Motivation

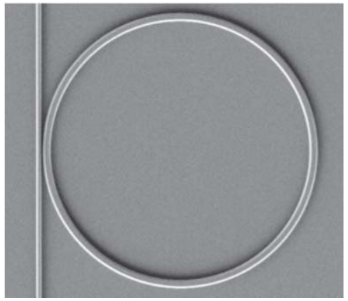
Scalable / robust all-optical logic gate

- ✓Same input / output wavelength
- ✓Simple design: Single cavity design

- ✓Study the effect of input power fluctuation
- ✓Study fabrication error tolerance

Calculation model - cavity -

Silicon nitride microring



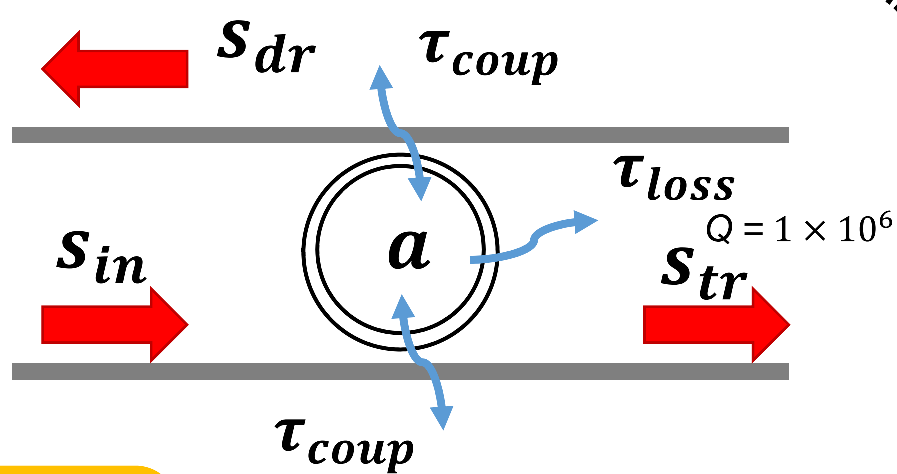
J. Levy, *et.al.*, Nature Photon. **4**, 38 (2010).

- High quality factor ($Q \sim 1 \times 10^6$).
- Large nonlinear refractive index ($n_2 = 2.5 \times 10^{-15}\,\mathrm{cm^2 W^{-1}}$)
- On-chip design

Modelling: Coupled mode theory

Resonant shift / Phase shift

$$\begin{cases} \frac{\mathrm{d}a}{\mathrm{d}t} = \left[j(\omega_0 - \omega) - \frac{1}{2}\left(\frac{1}{\tau_{loss}} + \frac{2}{\tau_{coup}}\right)\right] a + \sqrt{\frac{1}{\tau_{coup}}} \exp(j\theta)\, s_{in} \\ s_{\mathrm{tr}} = \exp(-j\beta d) \times \left[s_{in} - \sqrt{\frac{1}{\tau_{coup}}} \exp(-j\theta)\, a \right] \\ s_{\mathrm{dr}} = \exp(-j\beta d) \sqrt{\frac{1}{\tau_{coup}}}\, a \end{cases}$$



Kerr effect

$$\Delta \mathrm{n_{Kerr}} = \frac{2 n_2 c}{n_0} \frac{a^* a}{V} \qquad \delta\lambda = \frac{\Delta \mathrm{n_{Kerr}}}{n_0} \lambda_0$$

Resonant wavelength: 1550 nm & 1580 nm

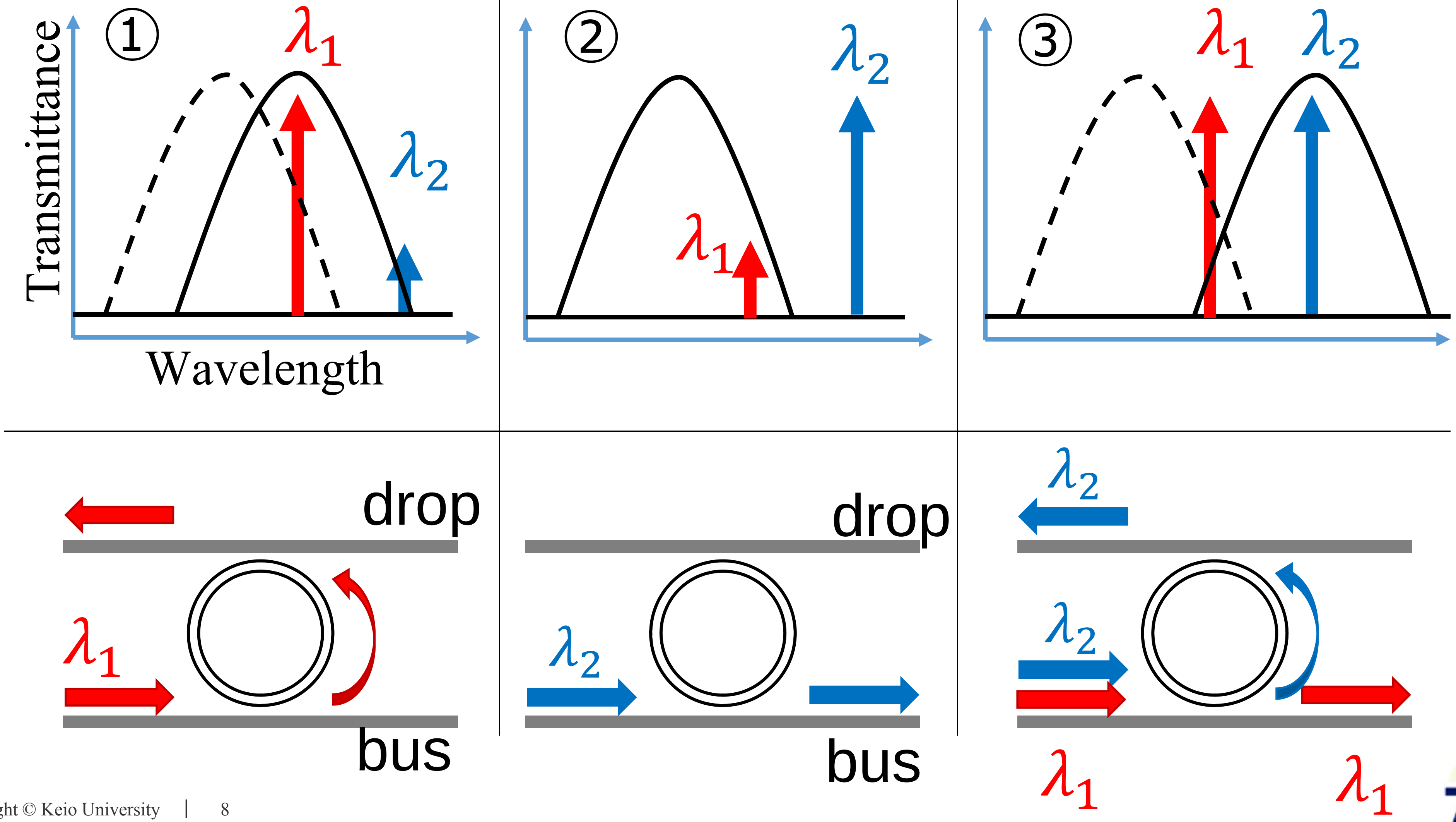
Signal light wavelength: 1550.1 nm & 1580.2 nm

Basic operation

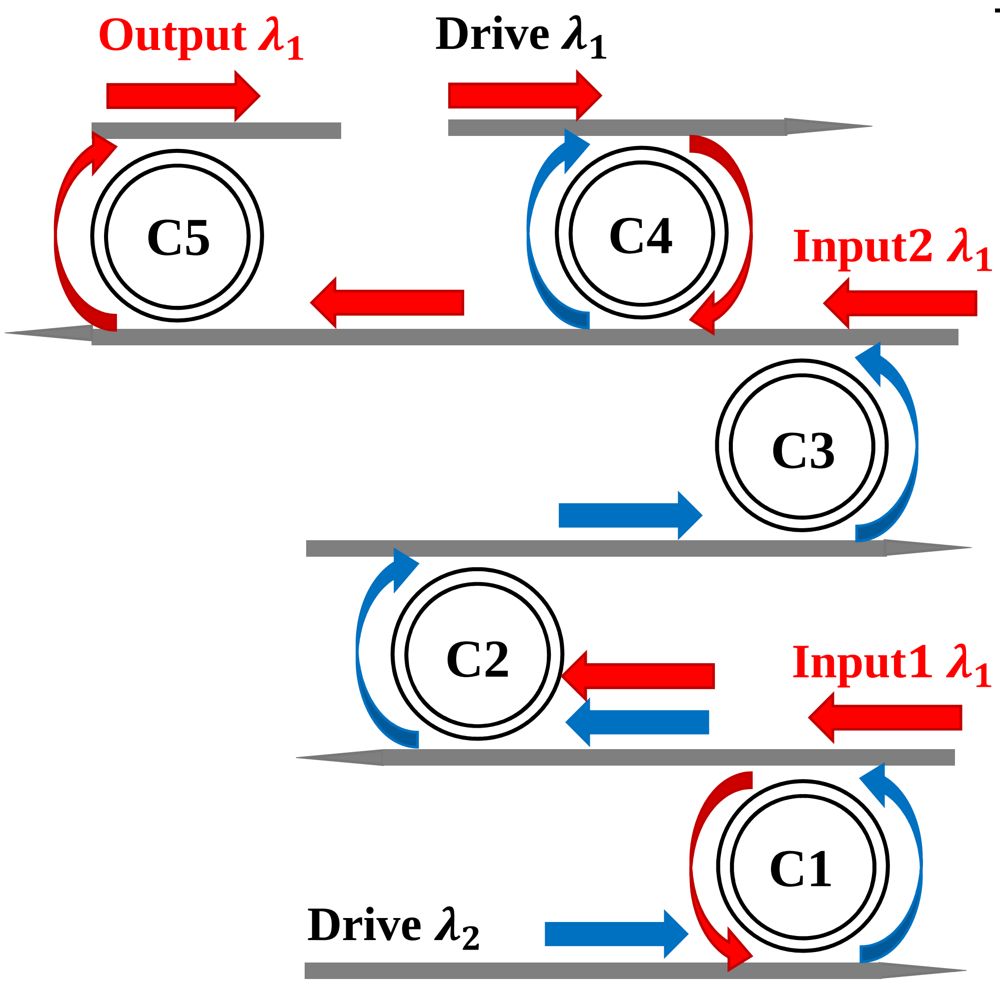
① Input only λ_1 ⇒ λ_1 drop

② Input only λ_2 ⇒ λ_2 pass through

③ Input λ_1 & λ_2 ⇒ λ_1 pass through & λ_2 drop



NAND gate design

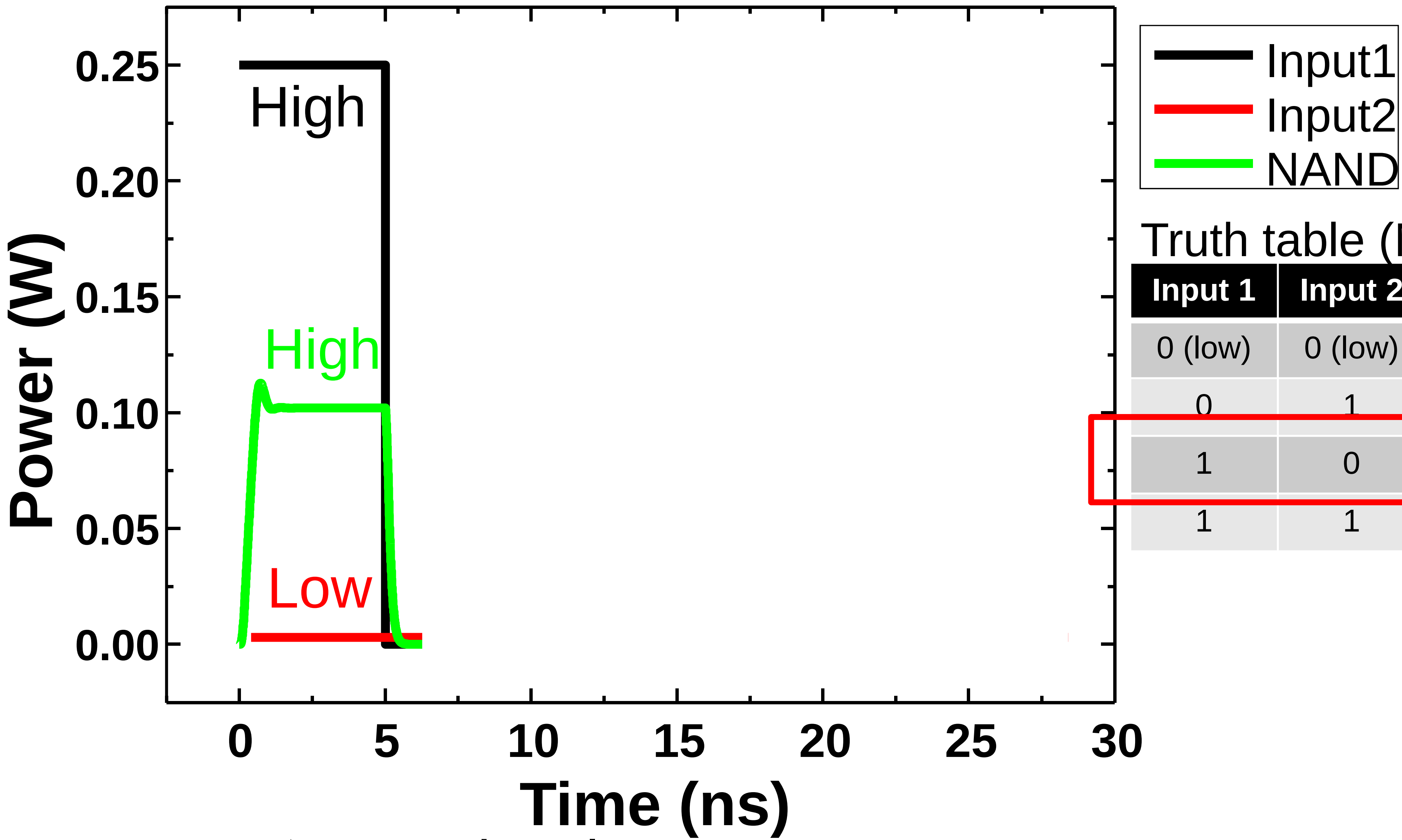


Design parameters:

	gap (nm)	Q_{couple}
C1	406	1.8×10^5
C2	375	1.2×10^5
C3	445	3.0×10^5
C4	445	3.0×10^5
C5	375	1.2×10^5

- ▶All cavities have the same design
- ▶Two inputs and one output have the same wavelength

NAND gate operation

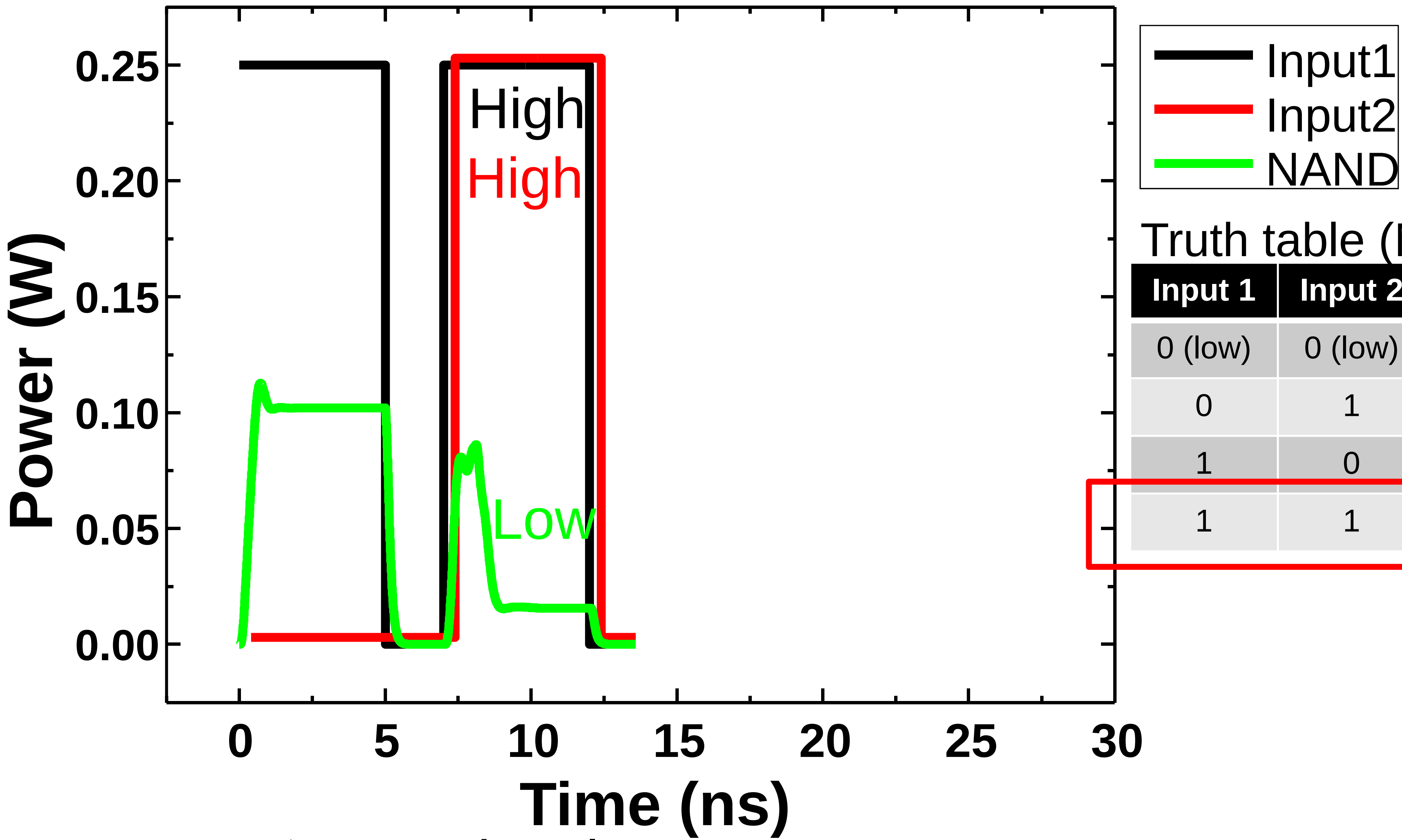


Truth table (NAND)

Input 1	Input 2	NAND
0 (low)	0 (low)	1 (high)
0	1	1
1	0	1
1	1	0

- RZ signal
- Input power = 250 mW

NAND gate operation



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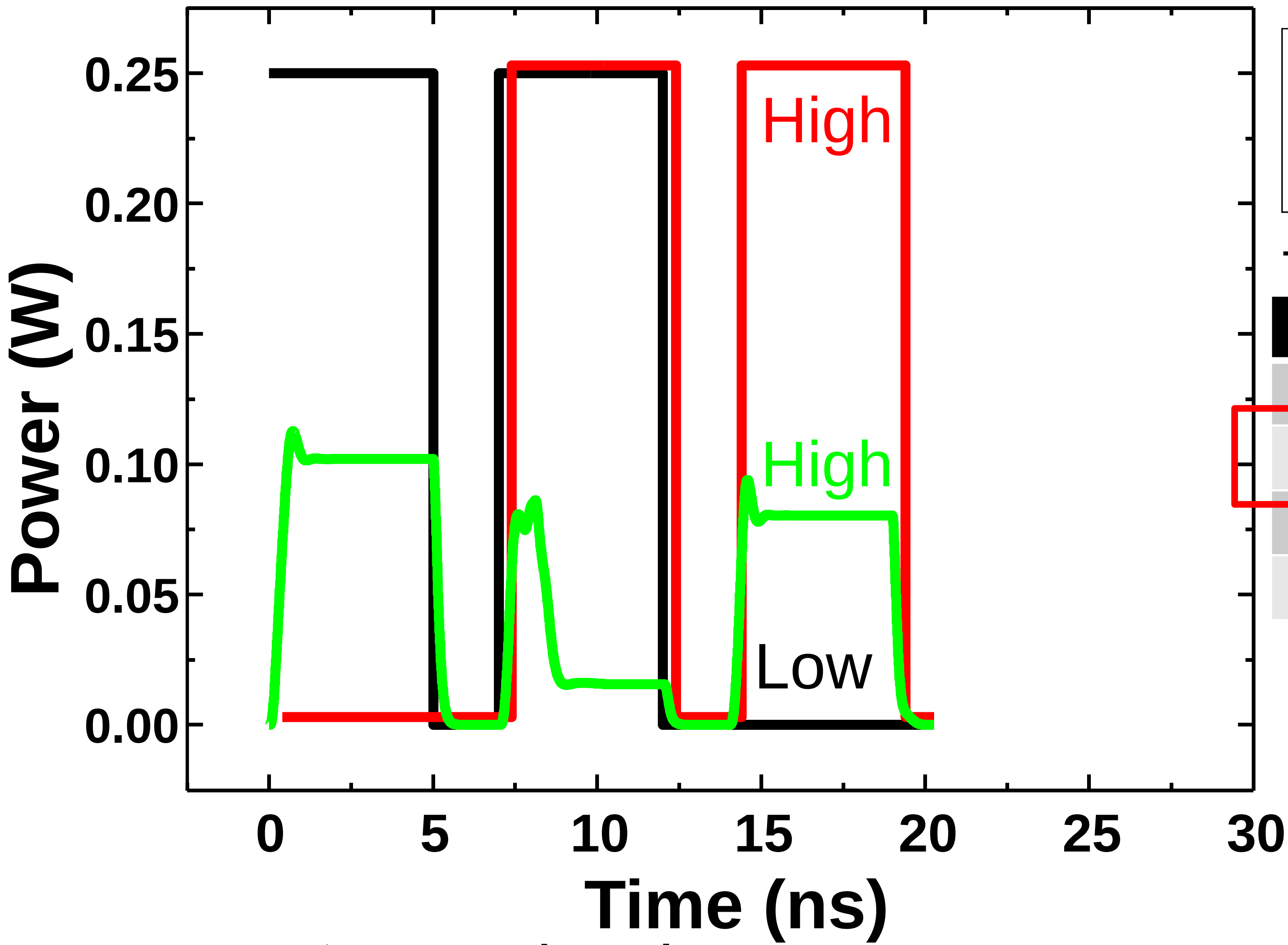
NAND gate operation



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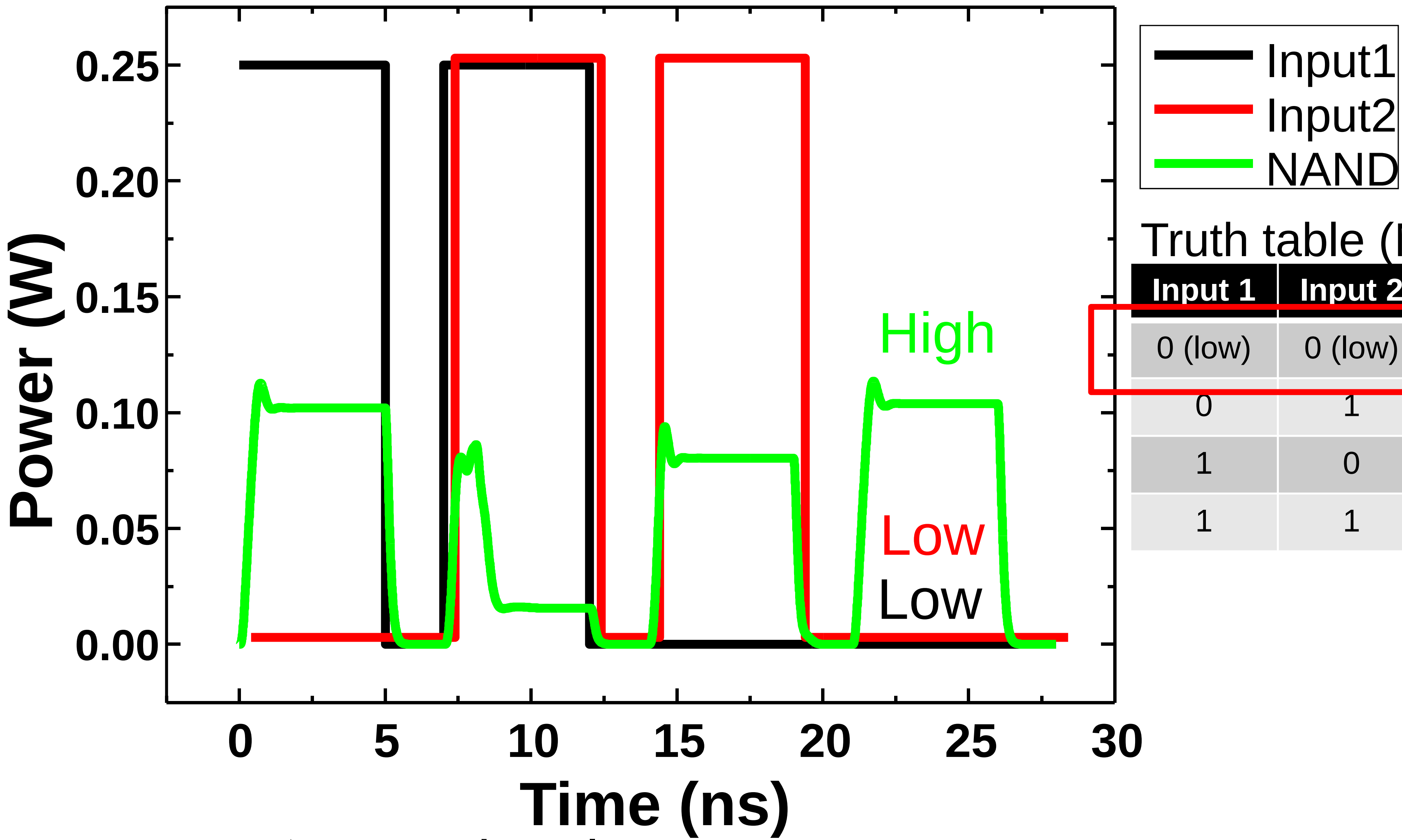
NAND gate operation



Truth table (NAND)

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0 (low)	0 (low)	1 (high)
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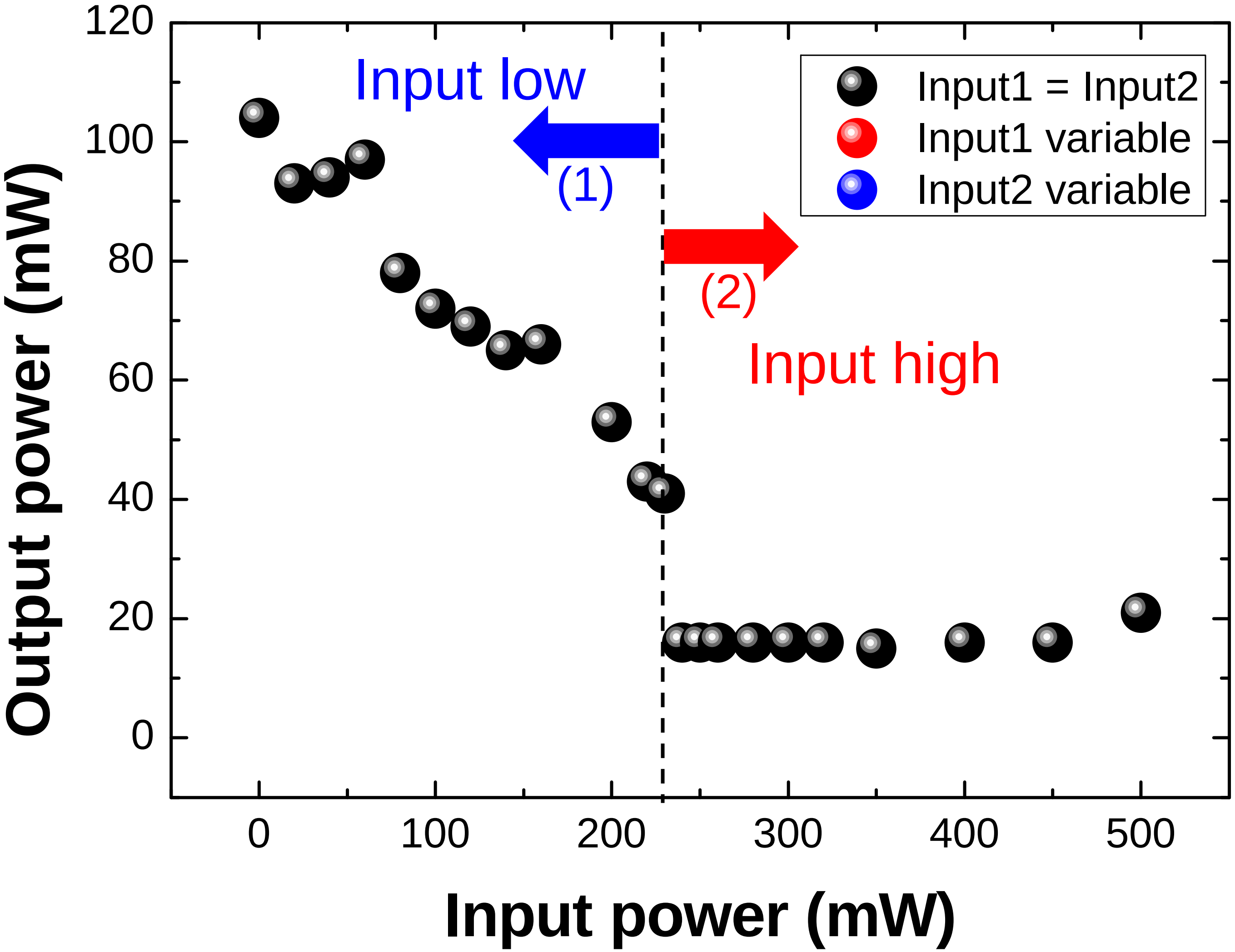
1	0	1
1	1	0

- RZ signal
- Input power = 250 mW

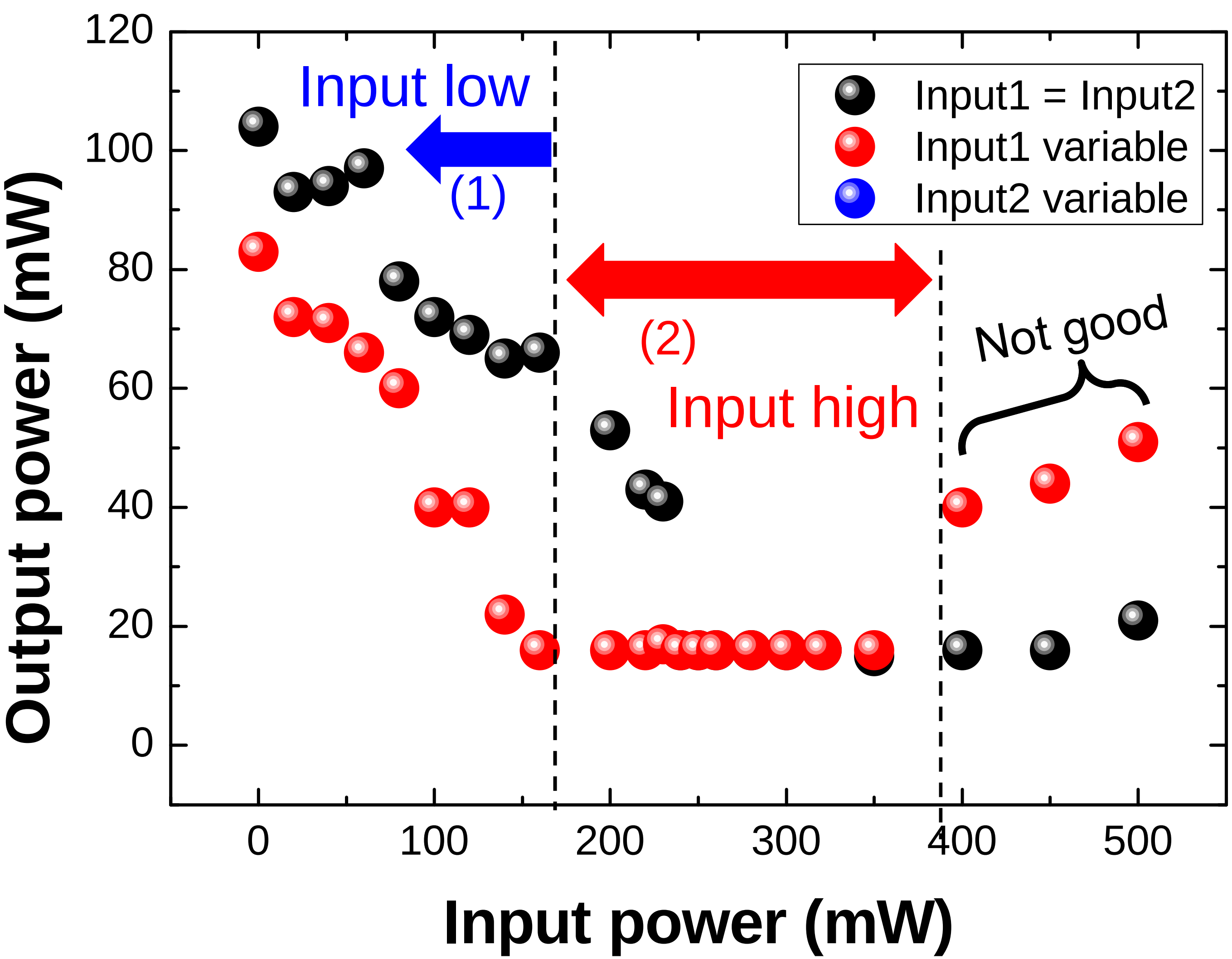
Power fluctuation tolerance



	Input 1	Input 2	NAND
(1)	0 (low)	0 (low)	1 (high)
	0	1	1
	1	0	1
(2)	1	1	0

Input low: 0〜230 mW
Input high: > 230 mW

Power fluctuation tolerance

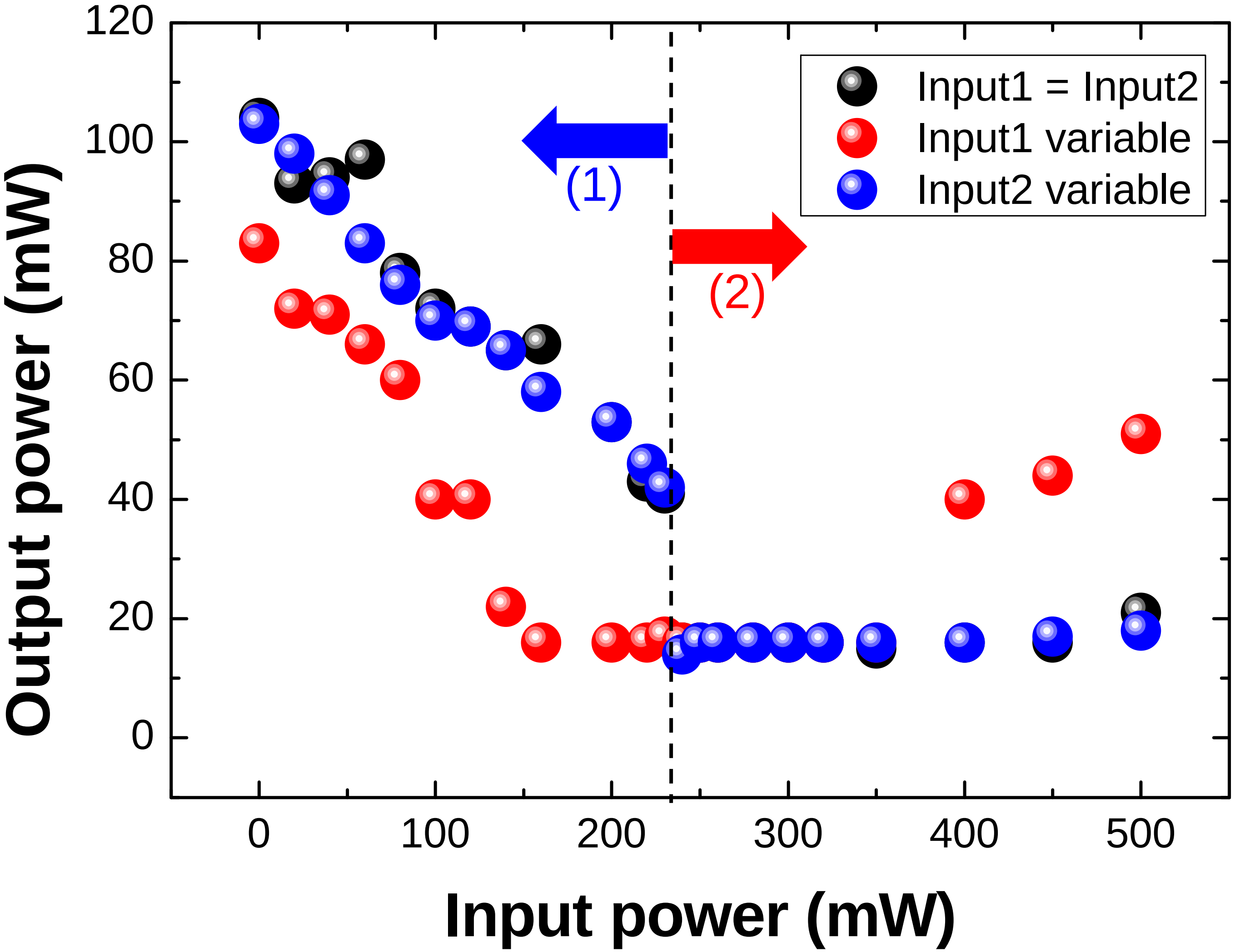


	Input 1	Input 2	NAND
	0 (low)	0 (low)	1 (high)
(1)	0	1	1
	1	0	1
(2)	1	1	0

(Input 2 is fixed at 250 mW)

Input low: 0～170 mW
Input high: 170～400 mW

Power fluctuation tolerance

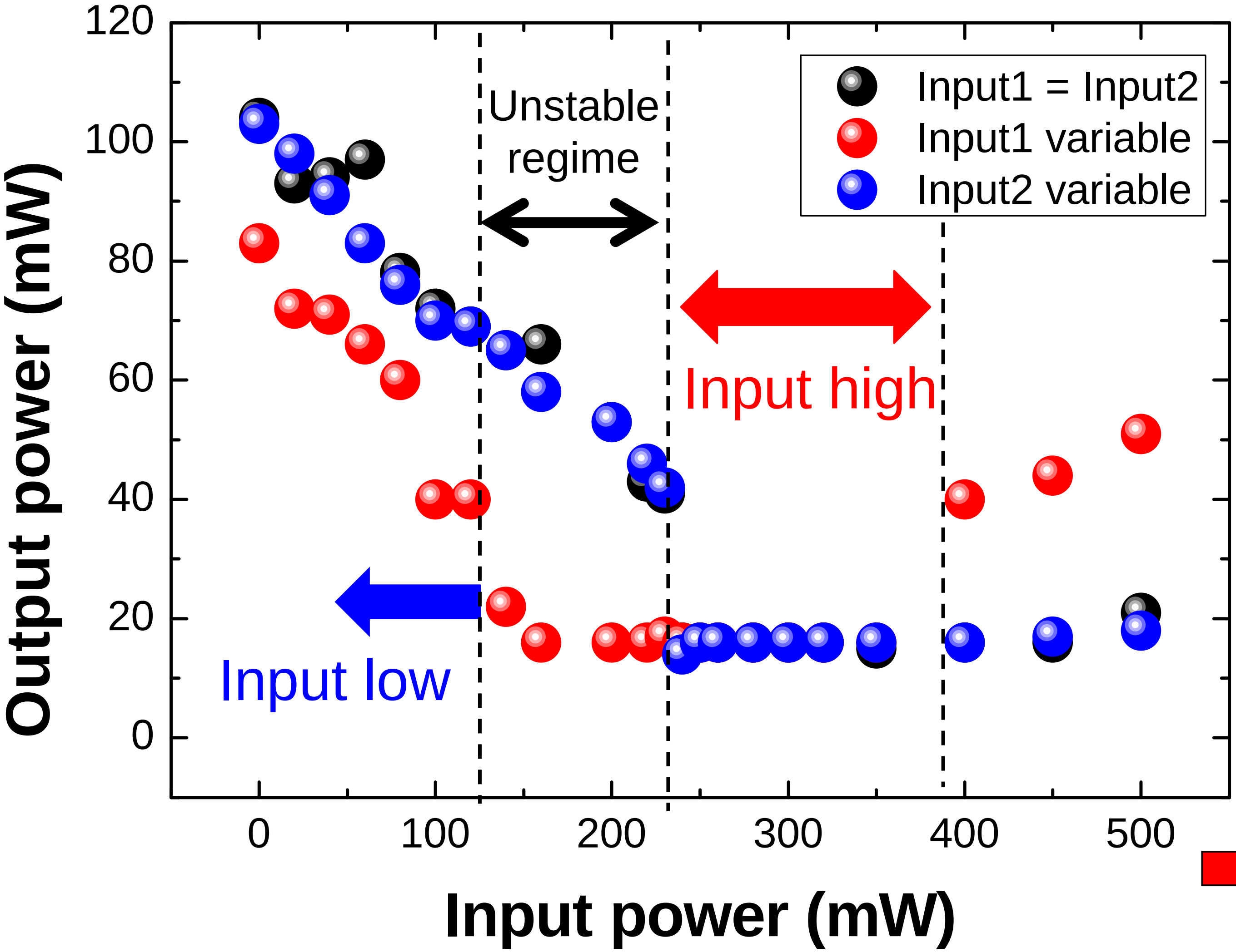


	Input 1	Input 2	NAND
	0 (low)	0 (low)	1 (high)
	0	1	1
(1)	1	0	1
(2)	1	1	0

(Input 1 is fixed at 250 mW)

Input low: 0～240 mW
Input high: 240～400 mW

Power fluctuation tolerance

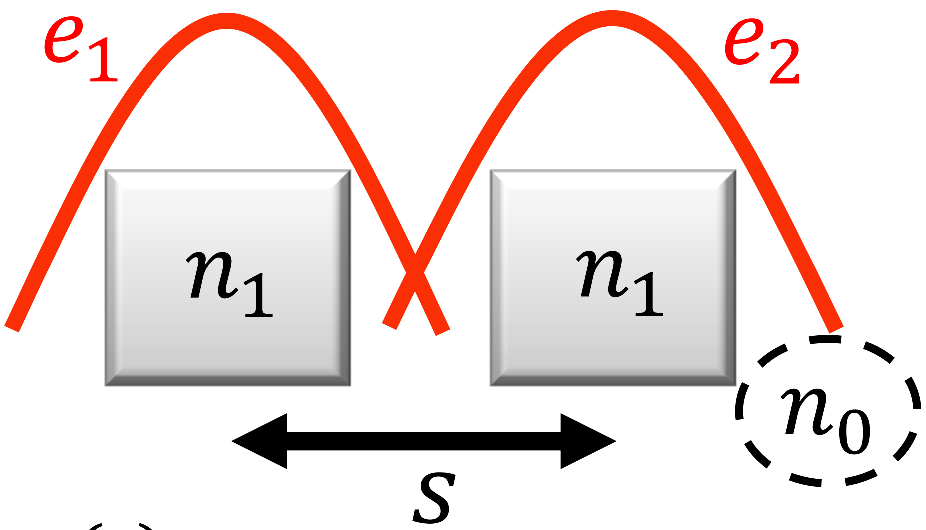


Input 1	Input 2	NAND
0 (low)	0 (low)	1 (high)
0	1	1
1	0	1
1	1	0

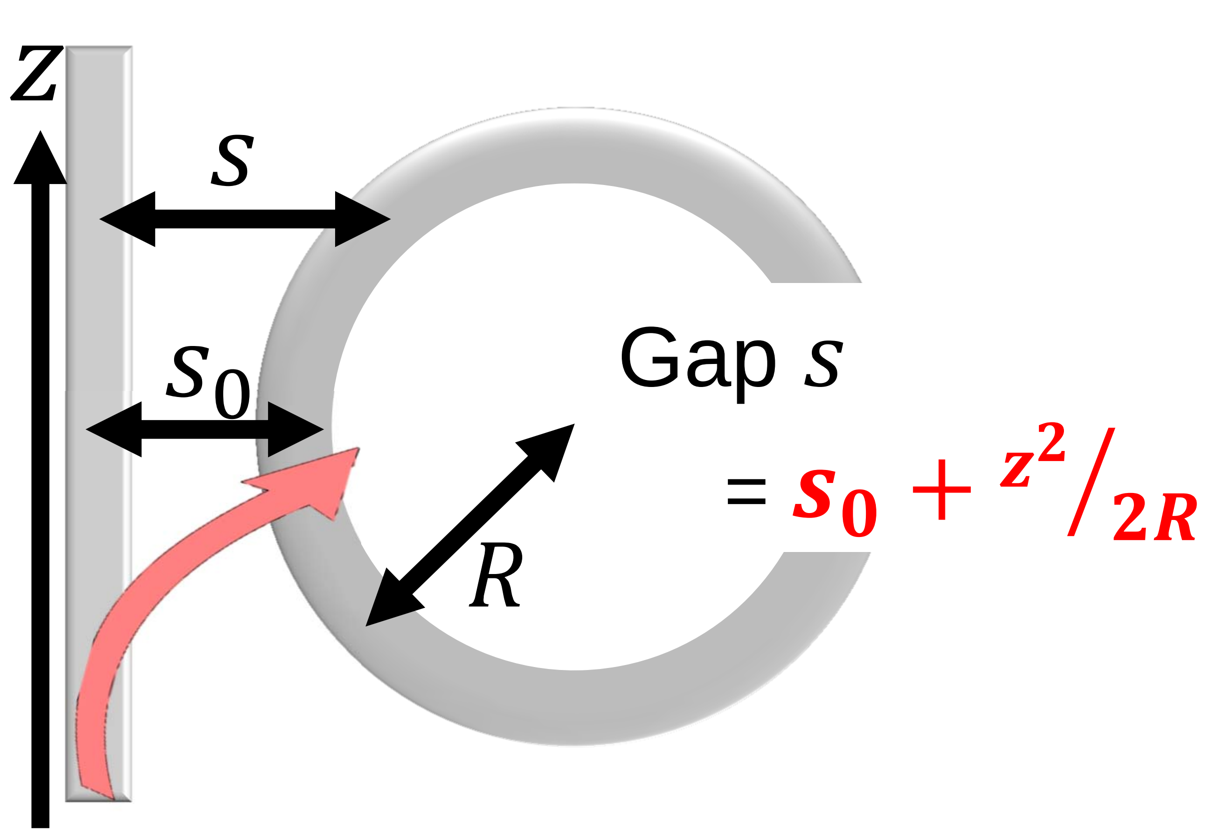
Input low: 0〜120 mW
Input high: 230〜400 mW

→ Stable > 100 mW range

Deriving Q_{couple} from gap distance



$$\kappa(s) = \frac{\varepsilon_0 \omega}{4} \int_{-\infty}^{\infty} (n_1^2 - n_0^2) e_1 e_2^* \, dx$$



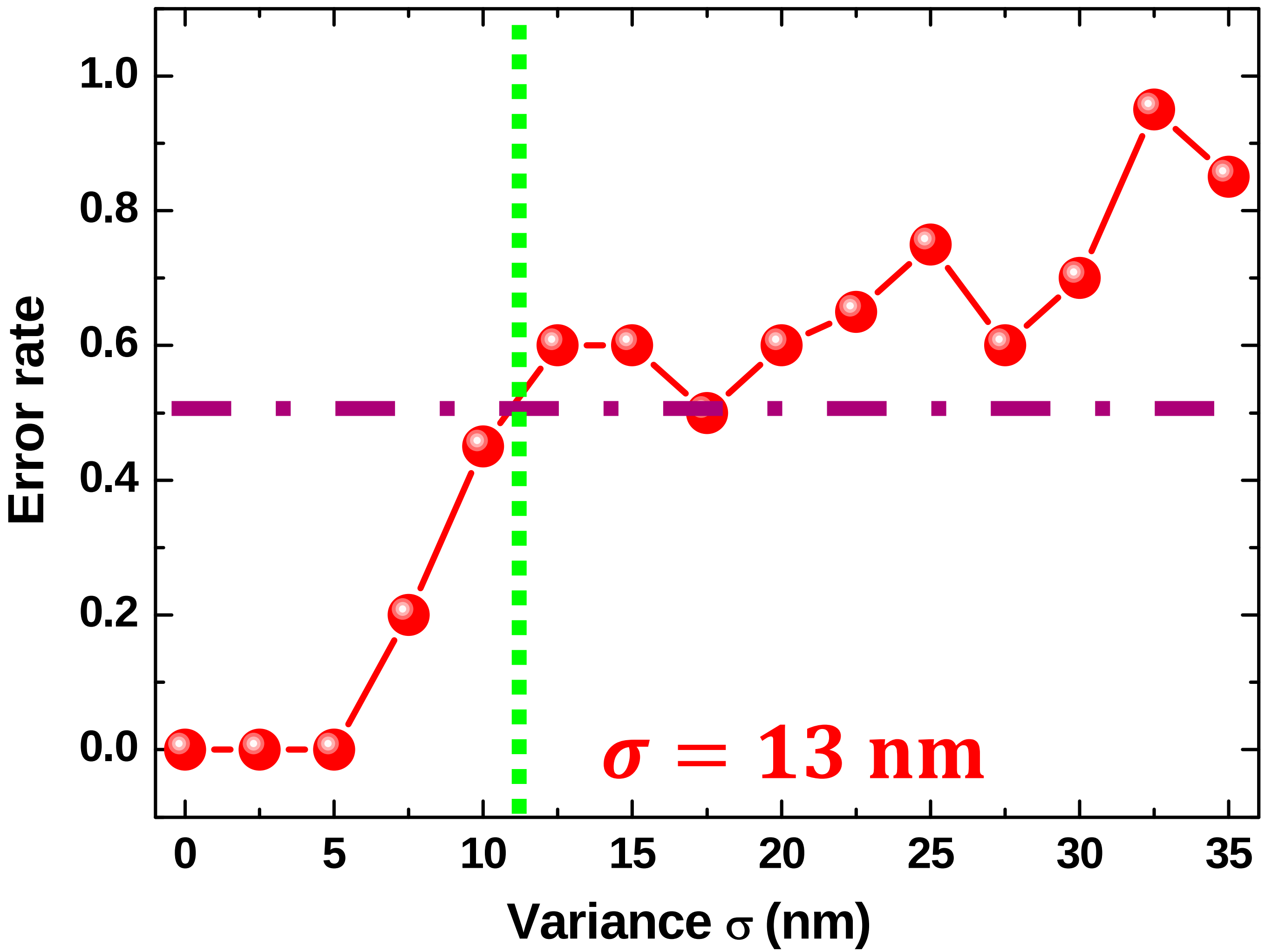
Coupling constant :

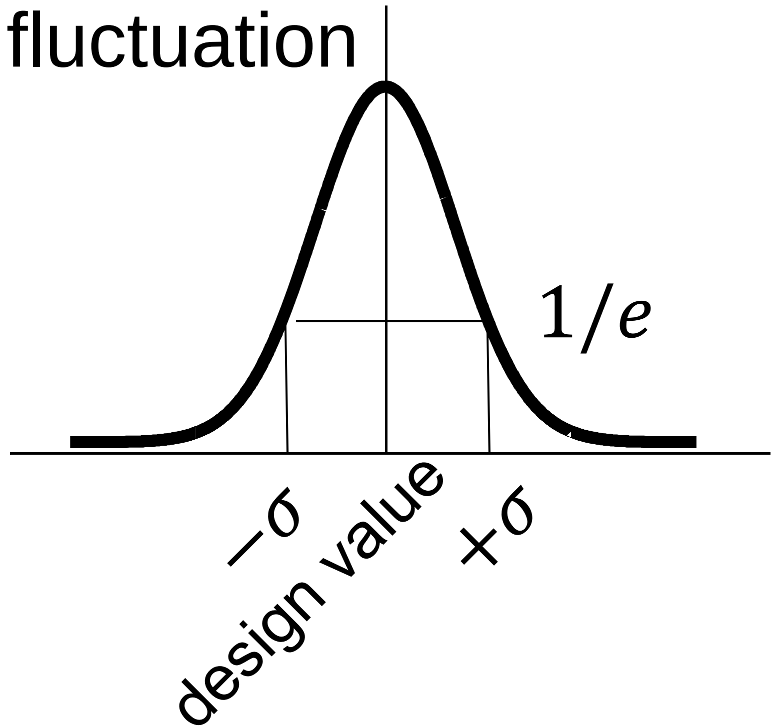
$$\kappa = \int_{-\infty}^{\infty} \kappa(s) \exp(-j\Delta\beta) \, dz$$

Gives κ from geometry s

$\Delta\beta = \beta_1 - \beta_2$:propagation constant difference

Gap distance flucturation





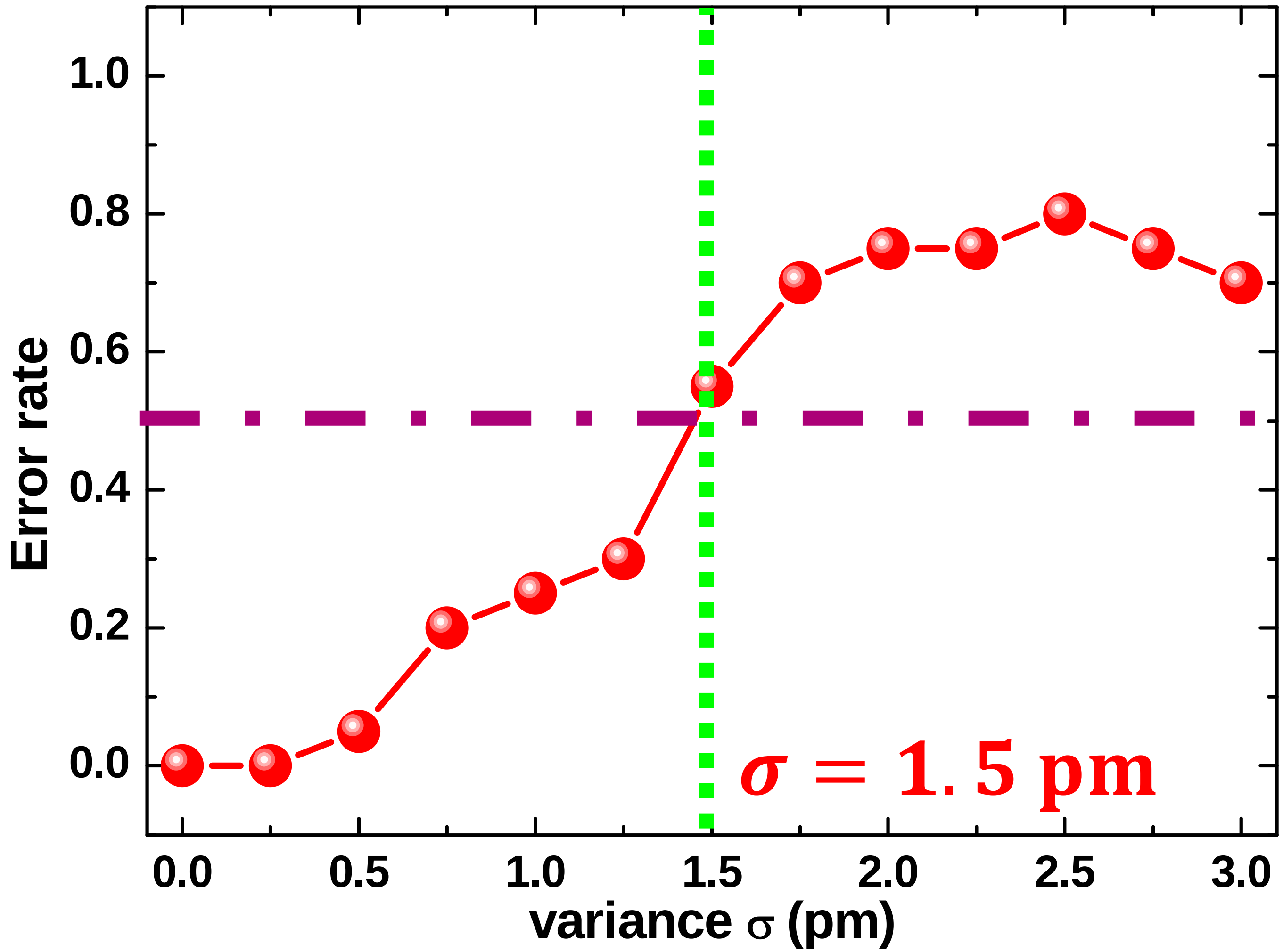
When σ is < 5 nm,
operation is error-free

Resonant wavelength flucturation

spectral width(HWHM)
> 5.0 pm

Fluctuation: 1.5 pm

Error rate is 50%



Summary & Future works

- Designed a scalable NAND gate.
- Studied the robustness: power / structure

- Error-free when the gap fluctuation is < 5 nm
- 50% error when the resonant wavelength fluctuation is 1.5 pm

Strong coupling will increase the tolerance

Our message:

Analysis on tolerance is important to put numerically study into practice

