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Robustness of scalable all-optical logic gates

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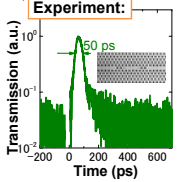
Keio University 1858 CALAMVS GLADIO FORTIOR

Background & Objective

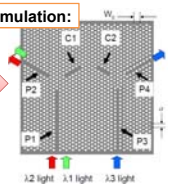
Experiment: Switch / bistable device consists of single cavity



T. Tanabe, *et al.*, Appl. Phys. Lett. **87**, 151112 (2005).

large gap

Simulation: Logic circuit consists of multiple cavities



A. Shinya, *et al.*, Opt. Express **14**, 3 (2006)

Problems

- Using >3 different wavelengths (No cascading possible)
- Using > 2 resonators w/ different designs
- Fabrication tolerance is unknown
- Robustness against input power fluctuation is unknown

Requirements for all-optical logics addressed by Prof. David Miller

- Cacadability & Fan-out
- Logic-level restoration
- Input &output isolation
- Absence of critical biasing
- Logic level independent loss
- fJ-level energy / ps-level speed
- 10-nm gate size

D. Miller, Nature Photon. **4**, 5 (2010).

Motivations

- **Design a system that satisfies above listed requirements (i.e. same in/out wavelength, single cavity design, no back-reflection …)**
- **Study the tolerance of the fabrication error**
- **Study the robustness against input power fluctuation**

Calculation model

Coupled mode theory (CMT)

Material SiN $n_0 = 1.98, n_2 = 2.5 \times 10^{-15}\mathrm{cm^2W^{-1}}$

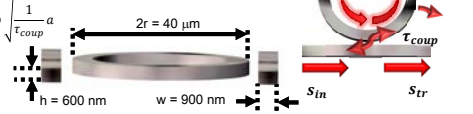
Waveguide 900 nm wide, 600 nm tall **Resonator** $Q = 1 \times 10^6$, $r = 20\ \mu\mathrm{m}$

$a, s_{in}, s_{tr}, s_{dr}$: mode amplitudes in cavity, input, bus output, and drop output.

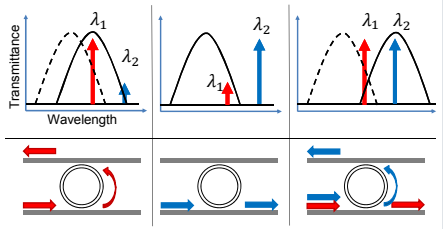
τ_{loss}, τ_{coup} : photon lifetimes of the cavity and the coupling to the waveguides

ω_0: resonant angular frequency, β: propagation constant, d : waveguide length

$$\begin{cases} \frac{da}{dt} = \left[j\omega_0 - \frac{1}{2}\left(\frac{1}{\tau_{loss}} + \frac{2}{\tau_{coup}}\right)\right] a + \sqrt{\frac{1}{\tau_{coup}}}\exp(j\theta)\, s_{in} \\ s_{tr} = \exp(-j\beta d) \times \left[s_{in} - \sqrt{\frac{1}{\tau_{coup}}}\exp(-j\theta)\, a\right] \\ s_{dr} = \exp(-j\beta d)\sqrt{\frac{1}{\tau_{coup}}}\, a \end{cases}$$



Operating principle (Kerr effect)



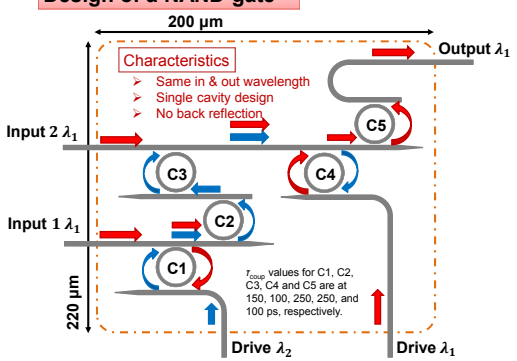
(a) λ_1 will drop (high) when only λ_1 is inputted (high).

(b) λ_2 will not drop (low) when only λ_2 is inputted (high).

(c) λ_2 will drop (high) when both λ_1 and λ_2 are inputted (high).

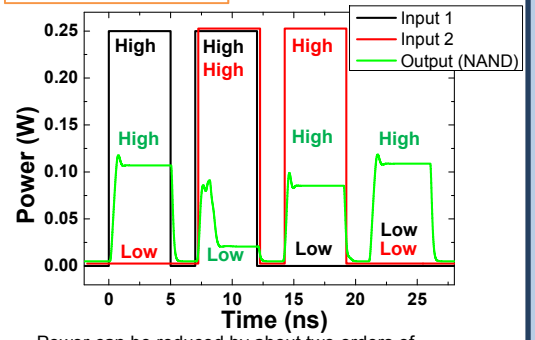
Operation of a scalable all-optical NAND gate

Design of a NAND gate



AND, NAND, OR gates are also designed

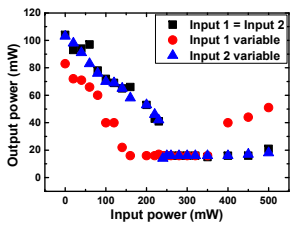
Input & output waveforms



Power can be reduced by about two orders of magnitude by employing the carrier-plasma dispersion effect in silicon microrings.

System robustness & fabrication tolerance

Input power fluctuation robustness



■ The output when the power of inputs 1 and 2 were changed together

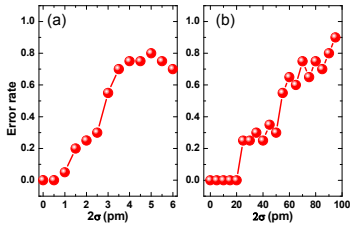
● The output when only input 1 was changed (input 2 is fixed at 250 mW)

▲ The output when only input 2 was changed. (input 1 is fixed at 250 mW)

Signal OFF range: 0 ~ 230 mW

Signal ON range: 230 ~ 350 mW

Resonant wavelength error tolerance



Output error rate of a NAND gate when C1-C5 cavities have different wavelengths

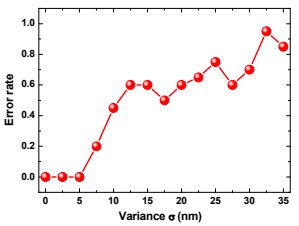
(a) Result for a NAND gate with optimized waveguide-cavity couplings.

⇨ The error rate is > 50% when 2σ is > 3.0 pm

(b) Result for a NAND gate with strong waveguide-cavity couplings.

⇨ With increased operation power, the threshold of 50% error is at 55 pm

Gap distance error tolerance



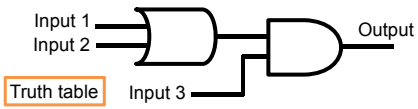
The output error rate is > 50% when $2\sigma'$ is > 12 nm

This value is within the range of state-of-the art fabrication technology.

τ_{coup} is analytically calculated from the gap distance and then CMT calculation is performed.

Cascaded operation

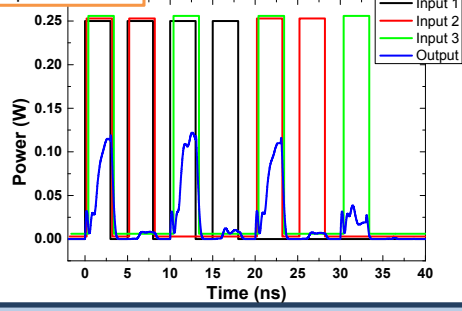
Logic circuit: OR & AND gates



Truth table

Input1	ON	ON	ON	ON	OFF	OFF	OFF	OFF
Input2	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Input3	ON	OFF	ON	OFF	ON	OFF	ON	OFF
Output	ON	OFF	ON	OFF	ON	OFF	OFF	OFF

Input & output waveforms



Summary

- **We designed all-optical logic system that have following characteristics:**
  - Same input & output wavelength
  - Same input & output signal format / restored output signal ⇨ Cascaded operation is possible
  - No back-reflection
  - Single cavity design
- **We investigate system robustness & fabrication tolerance of our system**
  - Less than 50% error with fabrication error of 12 nm.

Reference : A. Fushimi and T. Tanabe, "All-optical logic gate operating with single wavelength," Opt. Express, Vol. 22, No. 4, pp. 4466-4479 (2014).

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