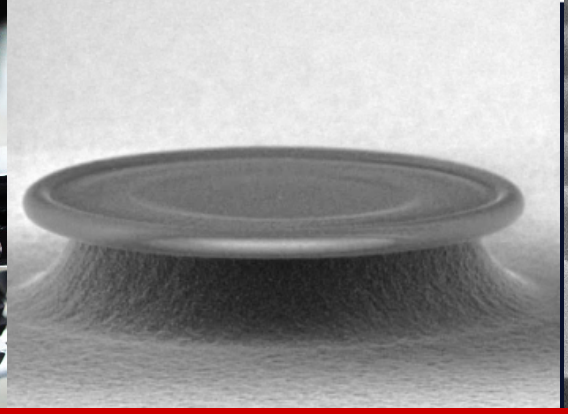
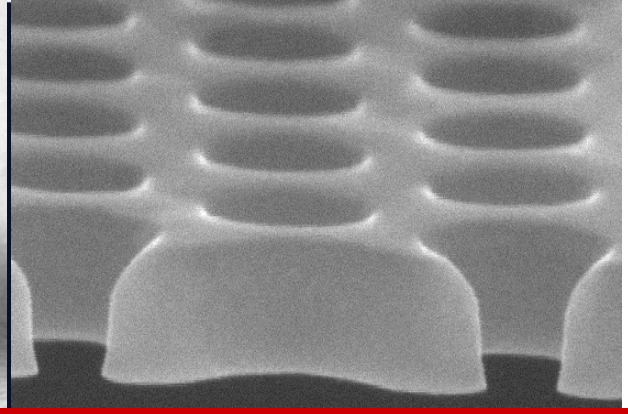
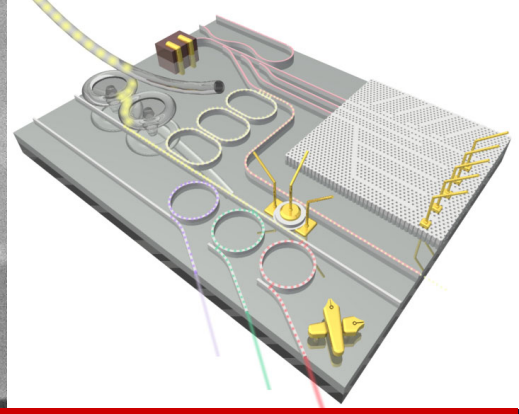





CLEO Pacific Rim 2018 2982117

Improved CMOS compatible photonic crystal demultiplexer

Keio University Graduate School of System Design and Management

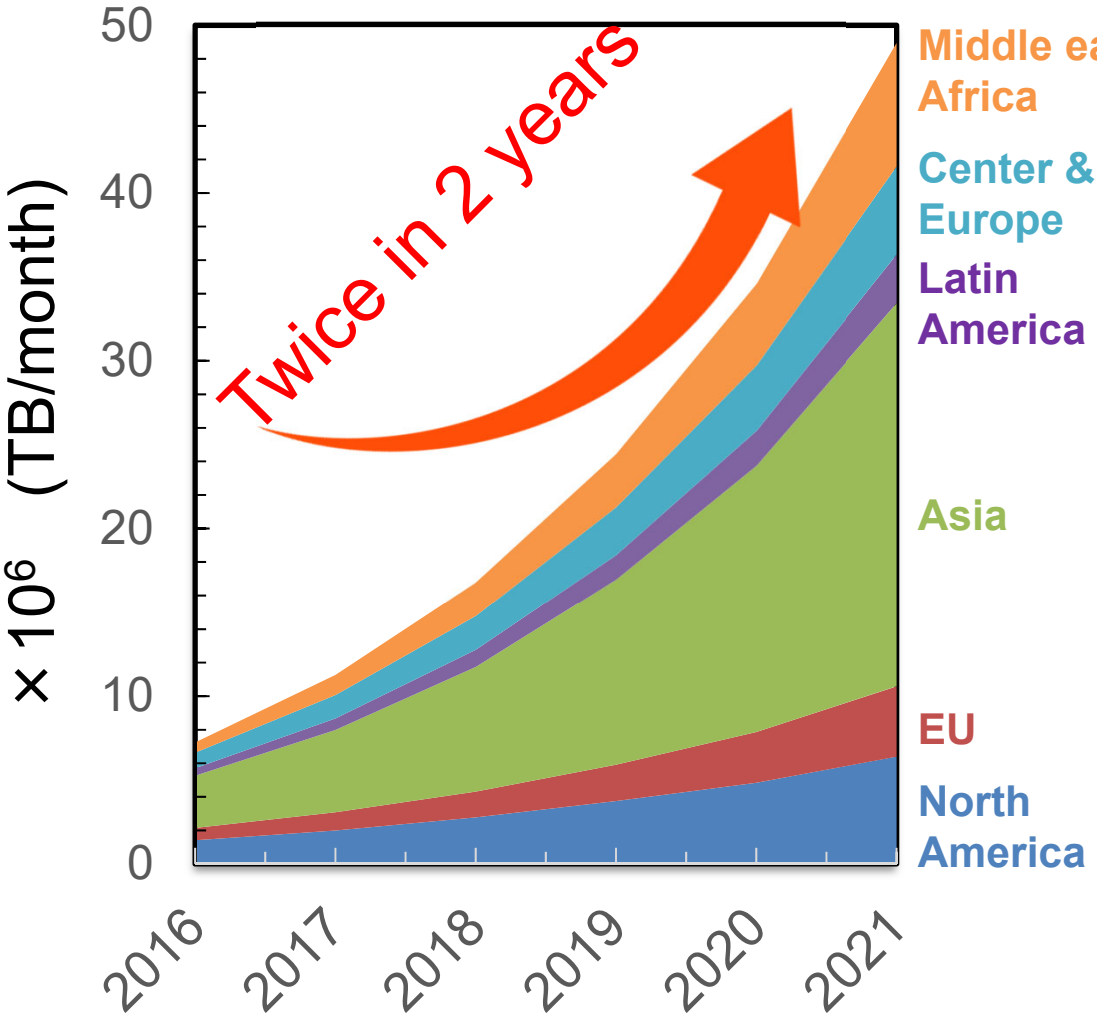
Shengji Jin, Yuta Ooka, Tomohiro Tetsumoto, Nurul Daud,

Naotaka Kamioka, Taku Okamura, Takasumi Tanabe

kins@phot.elec.keio.ac.jp

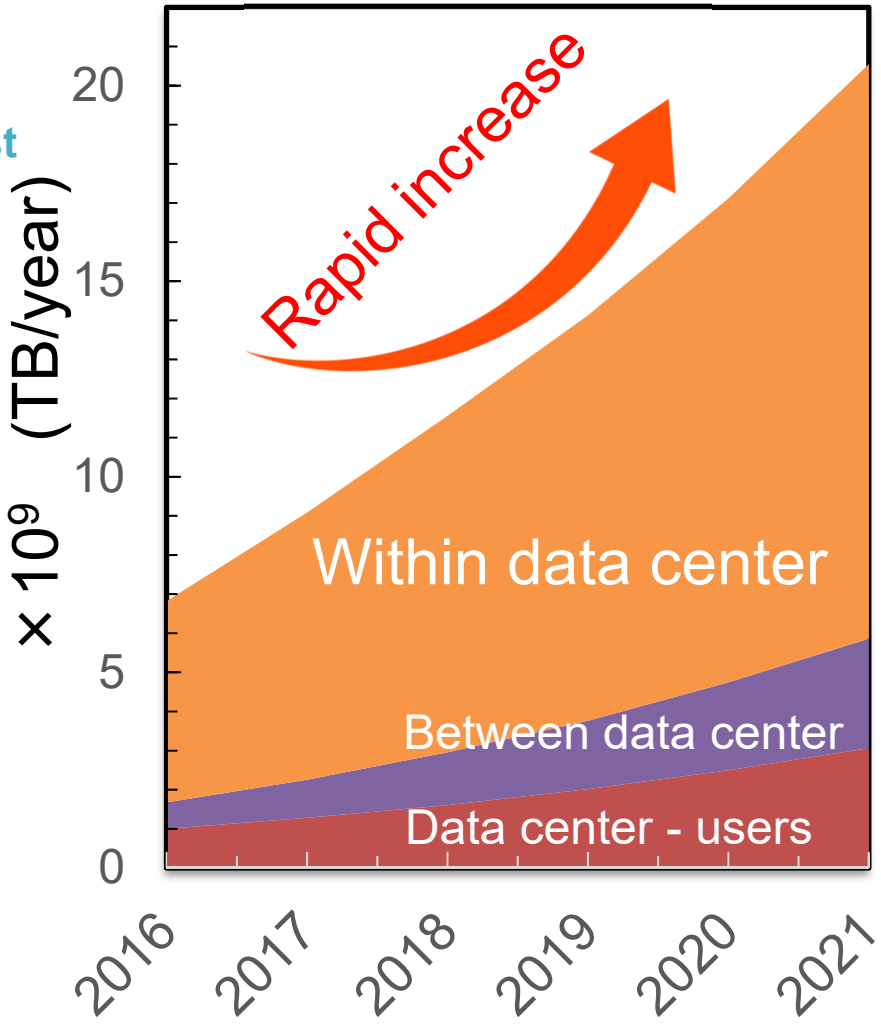
Data traffic estimation (mobile and data center)

➢ Mobile data traffic estimation



Cisco Visual Networking Index 2017

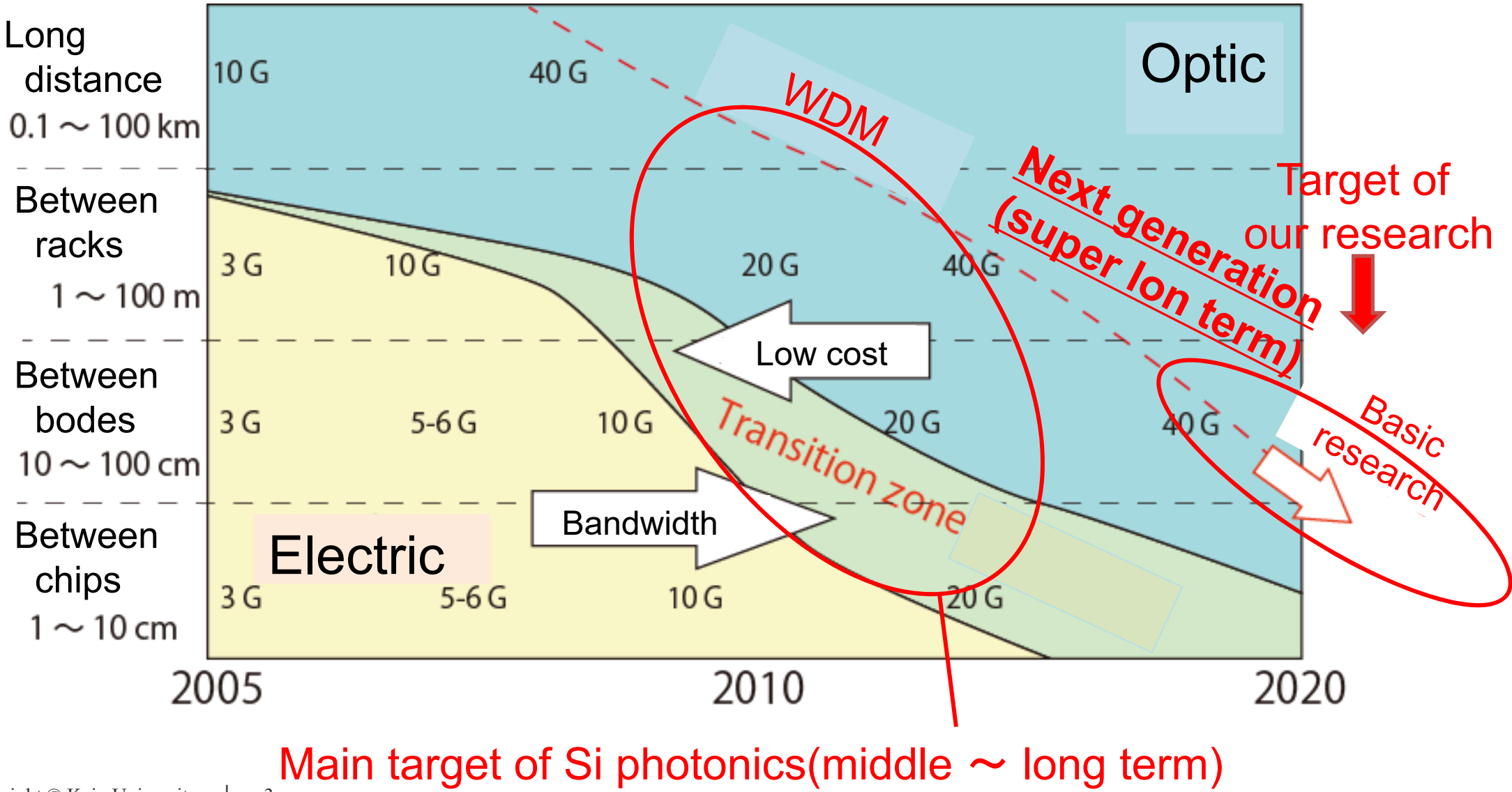
➢ Data traffic estimation in data center



Cisco Global Cloud Index 2017

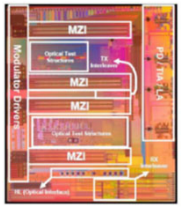
Shortening distance of optical telecom

J. Bautista, "The Potential Benefits of Photonics in the Computing Platform", Optoelectronic Integrated Circuits VII (SPIE, San Jose, CA, USA), pp. 1-8, 2005.

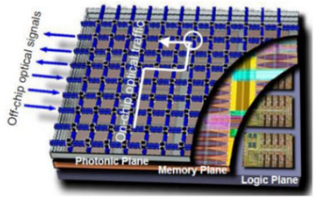


Trend and next-generation technology of Si photonics

➢ Si photonics devices

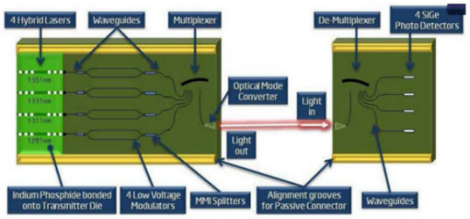


A. Narasimha, *et. al*, ISSCC 2007



Y. Vlasov, ECOC 2008 Tutorial, 2008

From the Finisar corp.'s website



A. Alduino, Intel, 2013

➢ Communication standard in DC

https://www.finisar.com/sites/default/files/resources/si_photonic_wdm_in_the_datacenter_2015.pdf?_ga=2.85209625.1695949495.1520763822-568920199.1520561408

Standard	Bit Rate	Fiber Pairs	λ	Baud Rate	Bits /Baud	Type
1GbE-LR, SR	1G	1	1	1G	1	Serial
10GbE-LR, SR	10G	1	1	10G	1	Serial
40GbE-SR4	40G	4	1	10G	1	Parallel
40GbE-LR4	40G	1	4	10G	1	WDM
100GbE-SR4	100G	4	1	25G	1	Parallel
100GbE-LR4, CWDM4, CL4	100G	1	4	25G	1	WDM
100G PSM4	100G	4	1	25G	1	Parallel

➢ Electric wiring vs. Optical wiring (Ultra short distance)

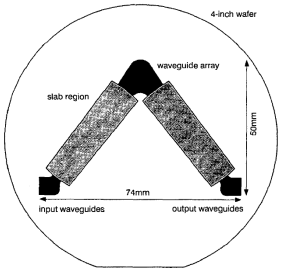
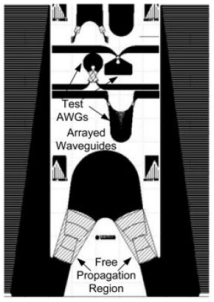
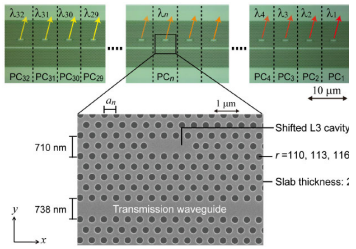
	Electric wiring	Optical wiring
Wiring width+pitch width	Cu **～100 nm** Co ～100 nm CNT < 100 nm	Si: **～um** (400 nm width + >1 um pitch)
Bandwidth	**< 3 GHz**	**> 10 GHz/ch**
Capacity / 1um wiring width	**～ 10 GHz**	**< 10 GHz/ch**

Wiring for short distance transmission

We need several channels to utilize advantages of optical wiring

⇒ Ultra compact DeMUX

Characteristics of various DeMUX

	PLC (silica)	Si - AWG	Si - PhC
DeMUX devices			
	Y. Hida, *et. al.*, OSA TOPS Vol. **54** Washington DC (2001)	Stanley Cheung, *et.al*, IEEE, Vol. **20**, (2014)	Y. Takahashi, *et. al.*, Opt. Exp. **22**, 4692 (2014)
Fabrication method	Photolithography	Photolithography	EB lithography
Number of channel	400	512	32
Channel spacing (GHz)	25	25	100
Device size (μm²/ch)	2.0×10^{7}	7.6×10^{4}	1.0×10^{2}
Productivity	○	△	×

Objective (Required properties of DeMUX)

I. **Size** : 100 μm^2 order

Ultra small size is ideal in terms of on-chip integration
→PhC or plasmonic circuits

II. **Number of channel**: ～10 ch (@ ～10 Gb/s per. ch.)

Around 10 ch would be needed to utilize optical wiring's advantages

III. **Crosstalk**: －10 dB ～ －20 dB

Our target is ultra-short distance and do not need EDFA
Around -20 dB would be enough

IV. **Total loss**: －10 dB

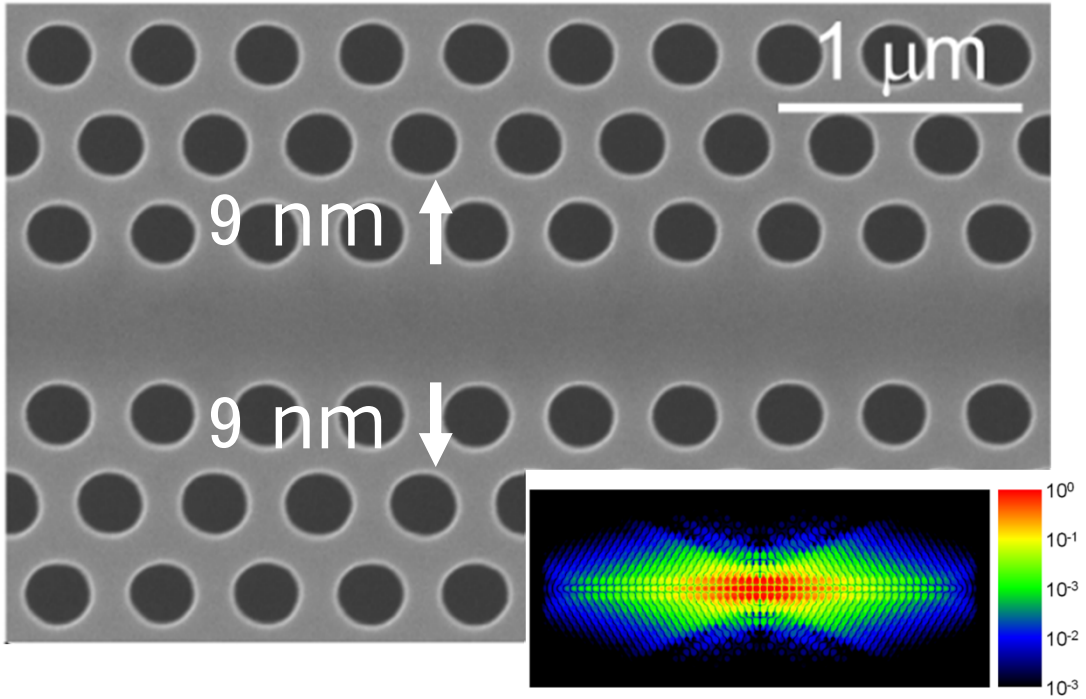
Micro strip line's transmission loss: ～ - 3 dB/cm
→ Around -10 dB loss@electrical@distance: ～cm
Optical wiring's loss: - 0.2 dB/cm → input loss is bigger

V. **Others**: Mass production(Photolithography)・Stability(SiO_2 cladding・heaters)

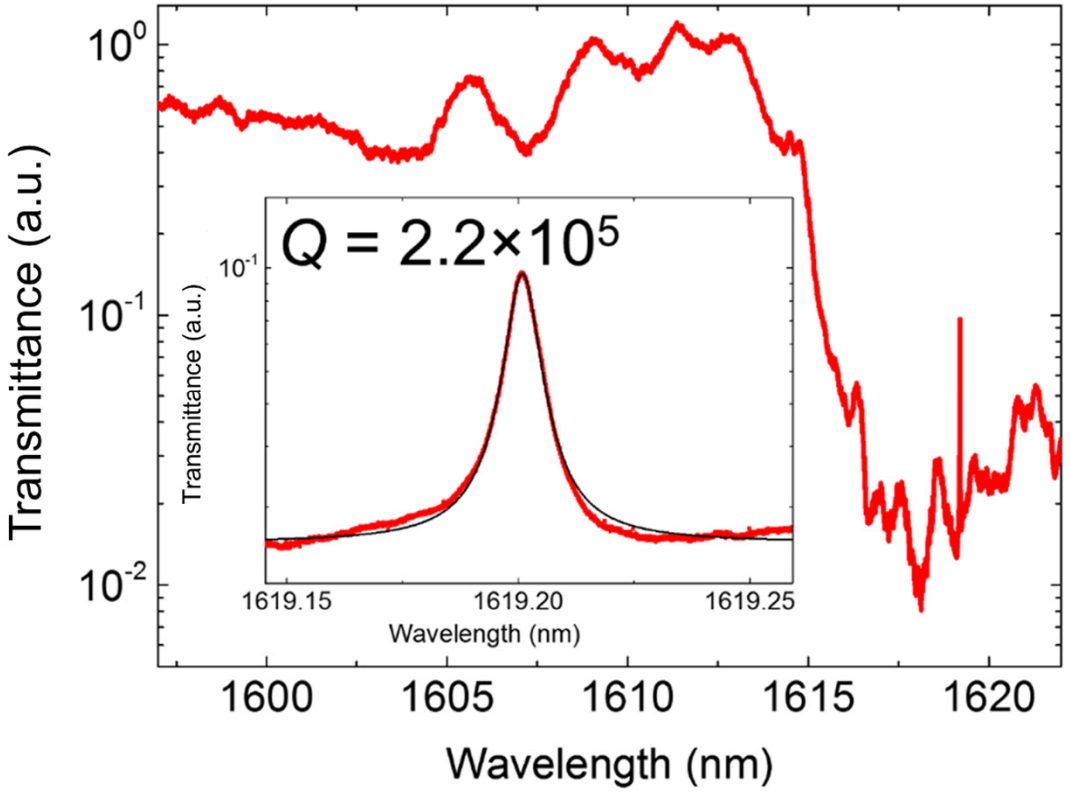
PhC DeMUX made by photolithography

CMOS compatible high Q PhC cavity

- High Q cavity



Y. Ooka, *et.al* Sci. Rep. **5,** 11312 (2015).



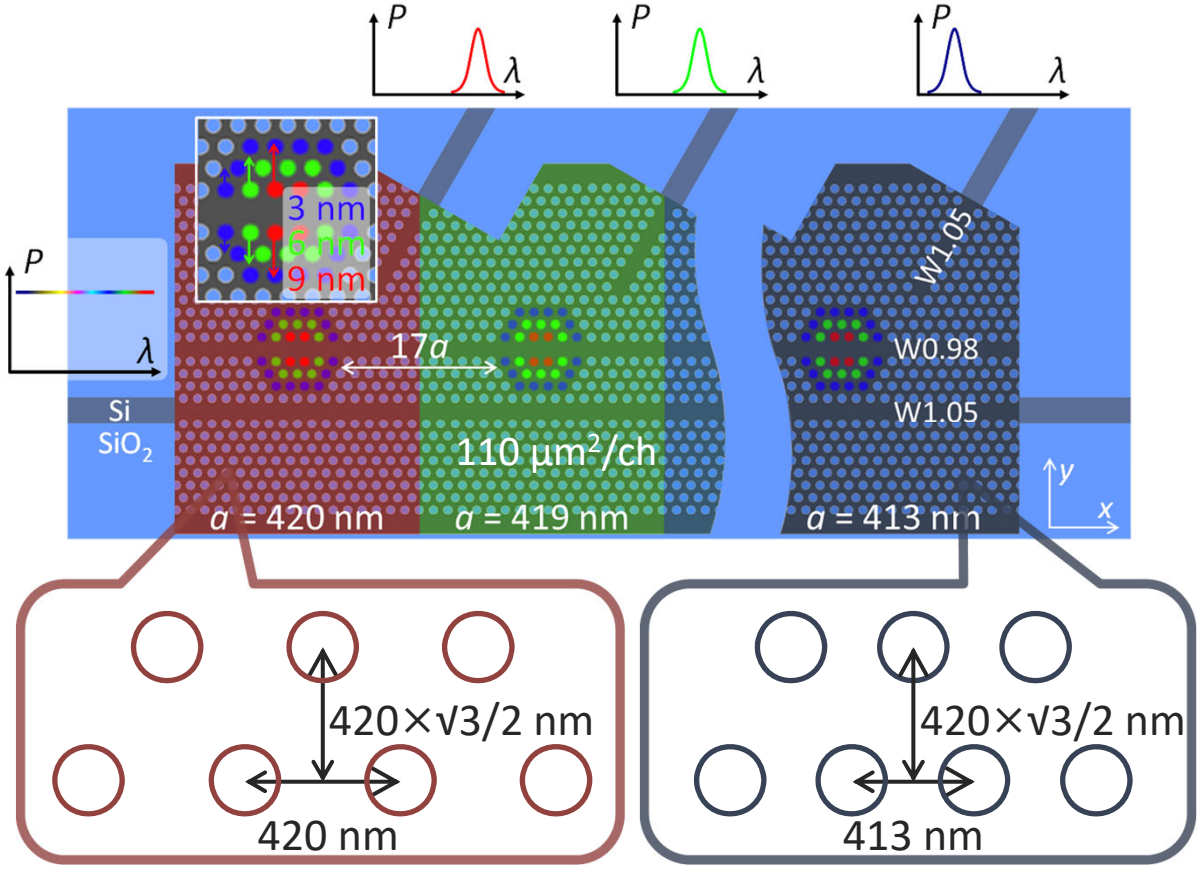
- **Photolithography**
- **SiO_2 cladding**

$$Q = 2.2 \times 10^5$$

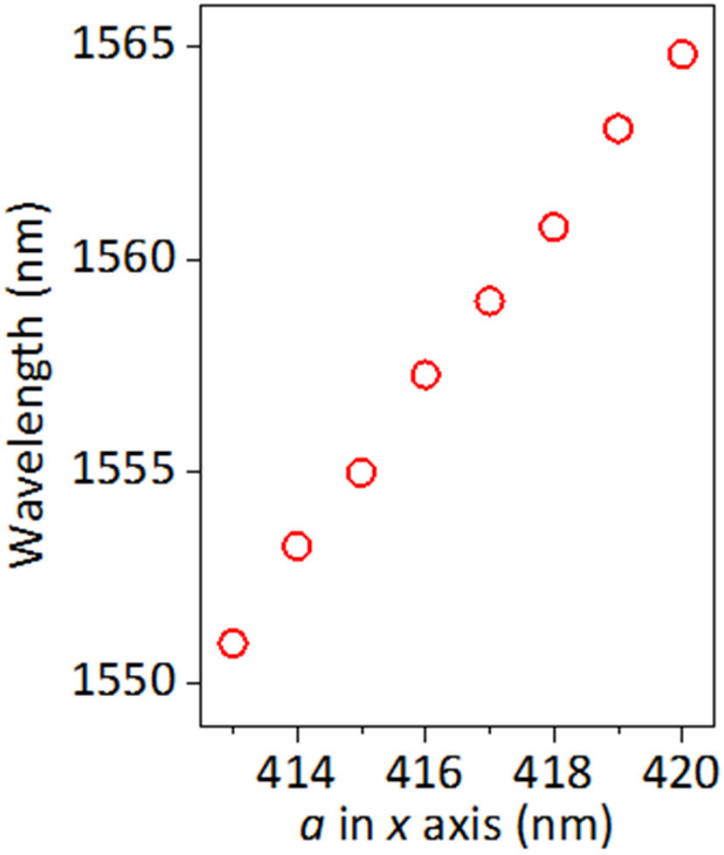
Design of DeMUX consisting of PhC cavity

Y. Ooka, *et al*. Opt. Express **25,** 1521 (2017).

➢ Design / upper view



➢ FDTD simulation



Changing lattice constant linearly

✓ lattice constant: 420 nm ~ 413 nm

✓ Number of channel: 8 ch

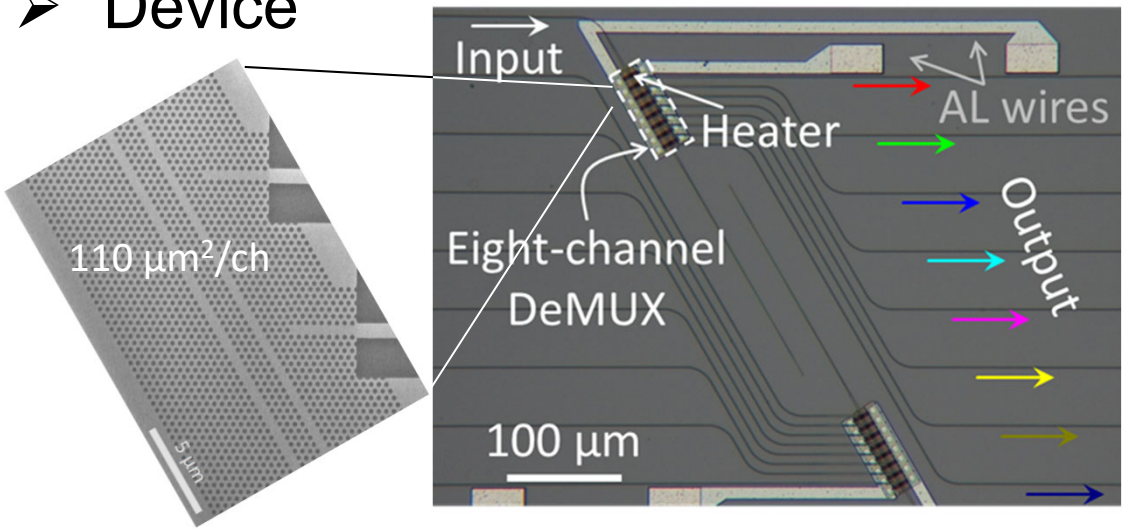
Fabrication of CMOS compatible DeMUX

Y. Ooka, *et al*. Opt. Express **25,** 1521 (2017).

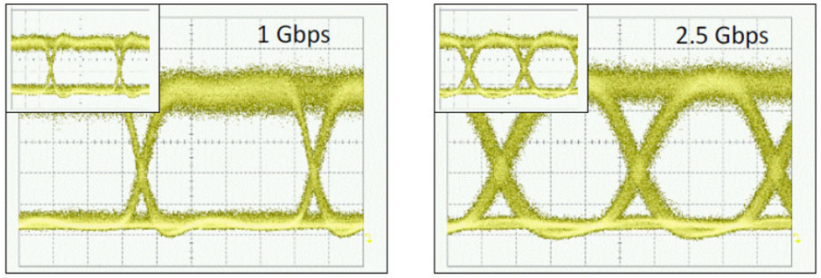
➢ Fabrication

- ✓ CMOS process foundry (IME in Singapore)
- ✓ 248-nm lithography (with phase-shifting mask)

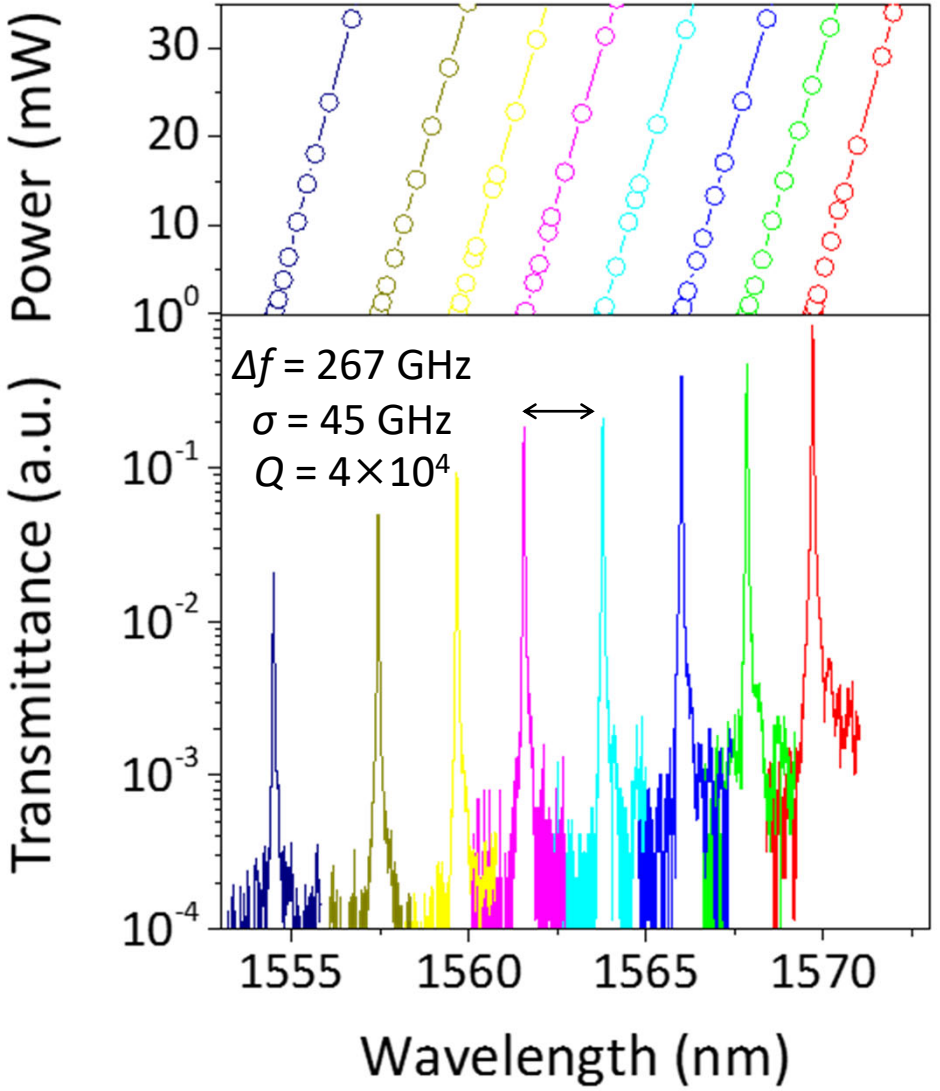
➢ Device



➢ Transmission property (1Gbps/2.5Gbps)



➢ Spectrum



Objective (Required properties of DeMUX)

I. **Size** : 100 μm^2 order

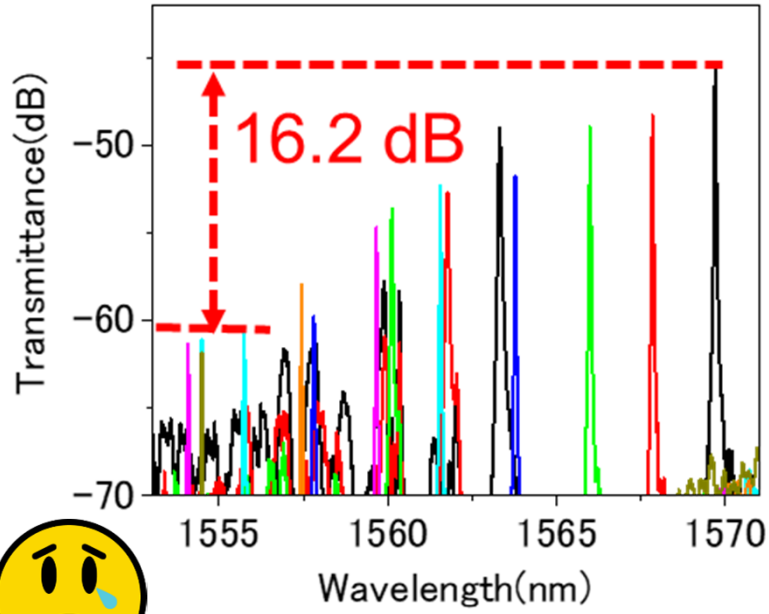
Ultra small size is ideal in terms of on-chip integra
→PhC or plasmonic circuits

II. **Number of channel**: ～10 ch (@ ～10 Gb/s per. ch

Around 10 ch would be needed to utilize optical wi

III. **Crosstalk**: －10 dB ～ －20 dB

Our target is ultra-short distance and do not need
Around -20 dB would be enough



Fluctuation (-16 dB)
Big loss(- 30 dB)

IV. **Total loss**: －10 dB

Micro strip line's transmission loss: ～ - 3 dB/cm
→ Around -10 dB loss@electrical@distance: ～

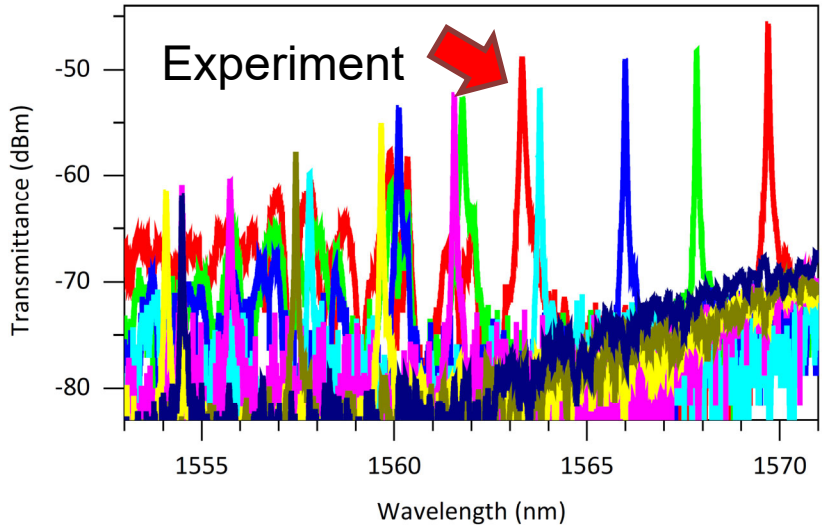
Optical wiring's loss: - 0.2 dB/cm → input loss is bigger

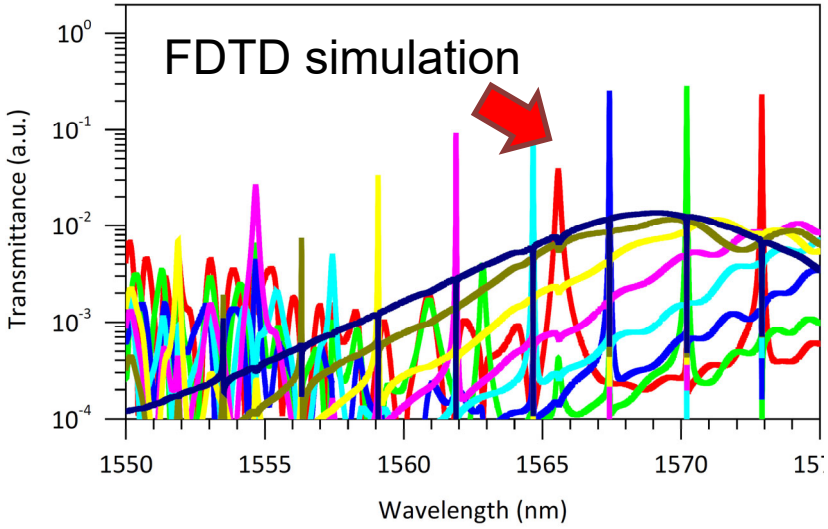
Others: Mass production(Photolithography)・Stability(SiO_2 cladding・heaters)

PhC DeMUX made by photolithography

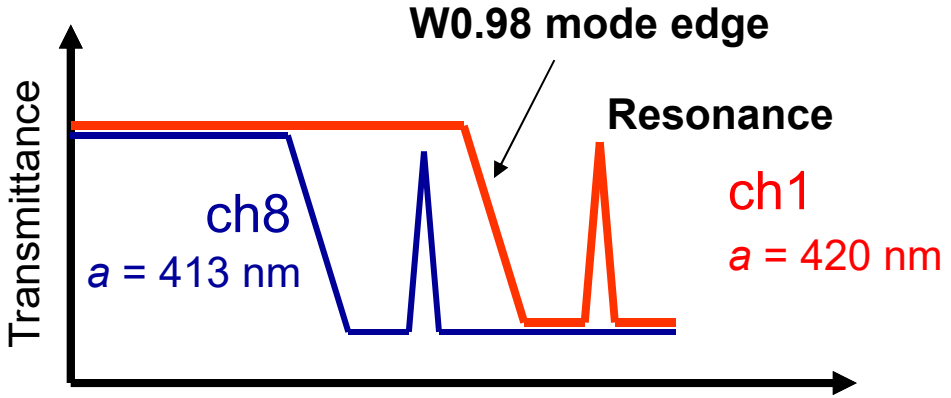
Cause of crosstalk

➢ Undesirable crosstalk

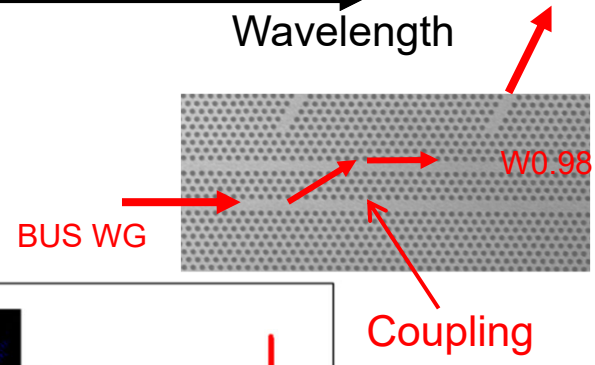


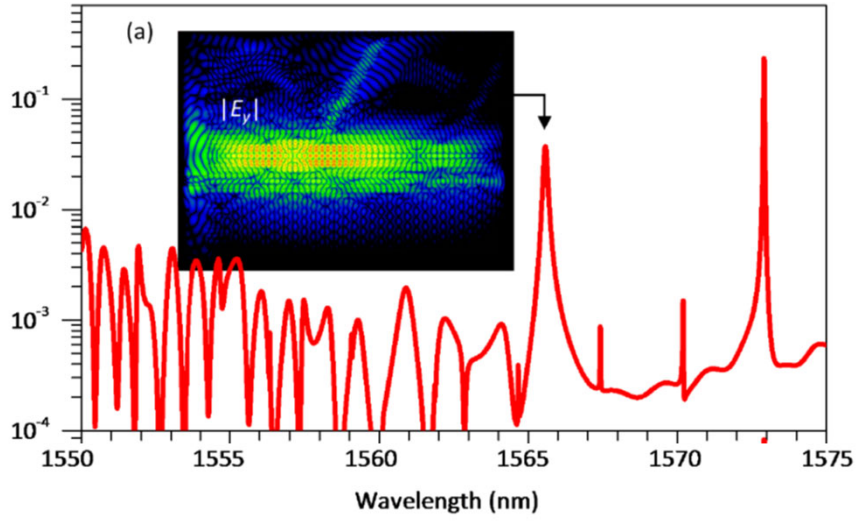


➢ Influence of mode edge



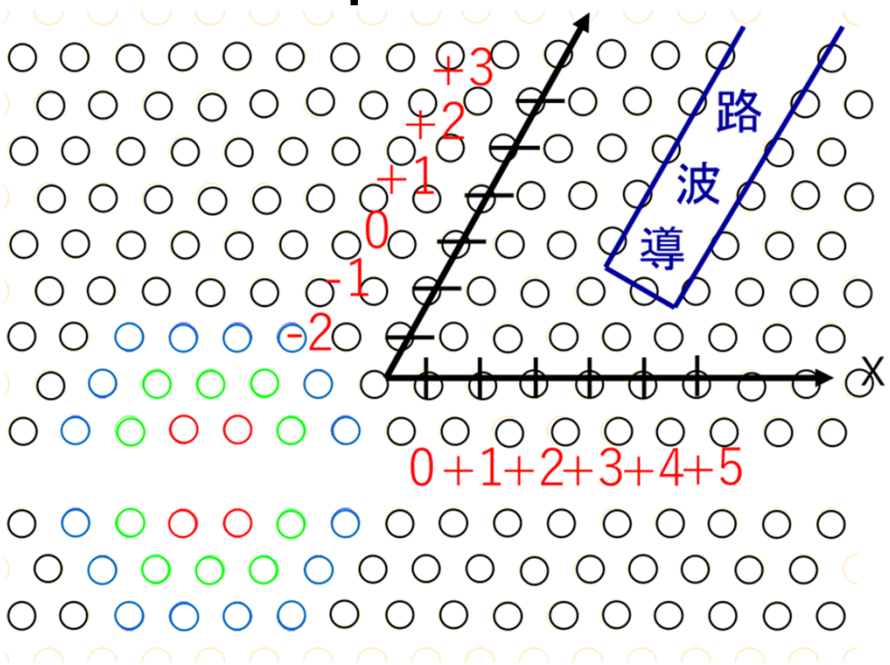
Problem:
Mode edge may coupe to PhC cavity





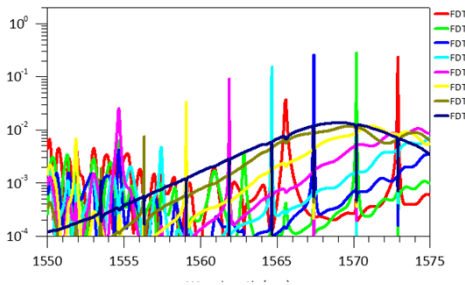
Optimization of output waveguides' position

➢ Position of output WG

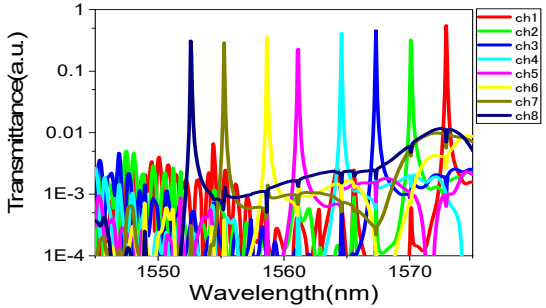


➢ FDTD simulation (Optimized results)

(x,y)=(0,0)

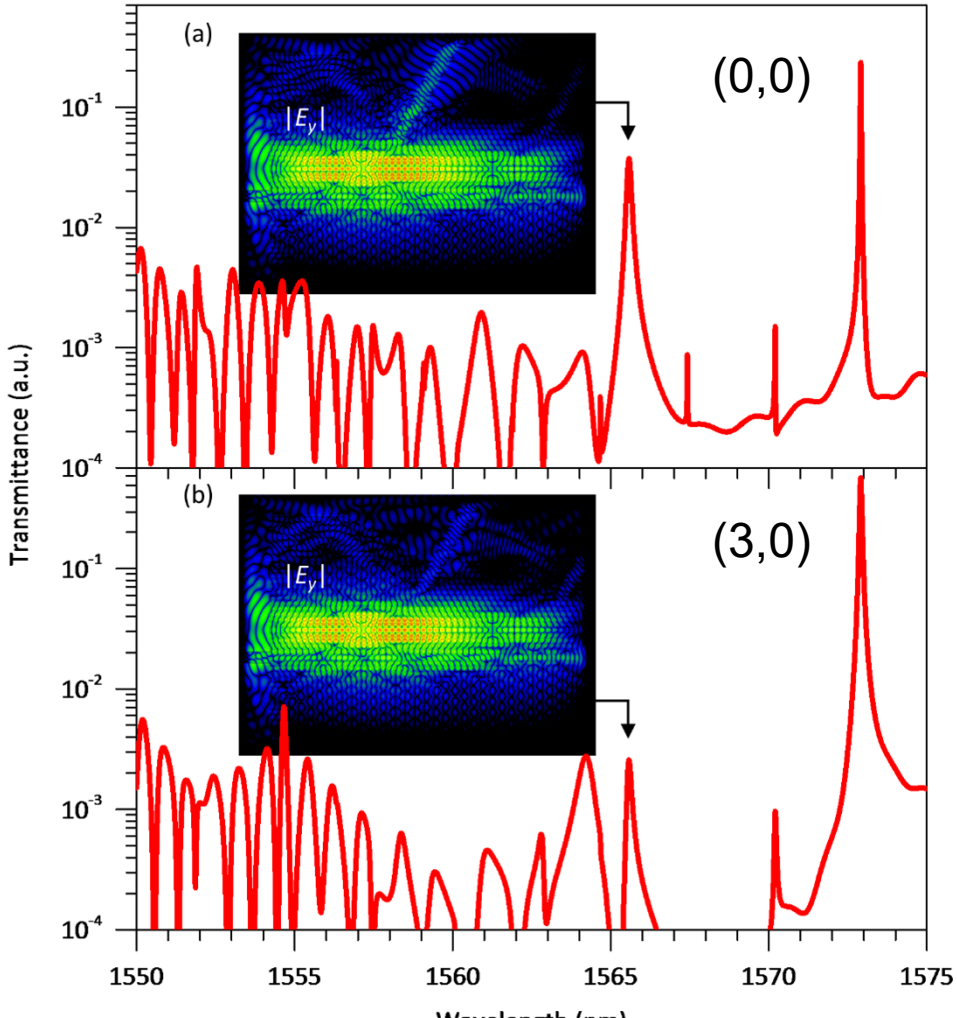


(x,y)=(3,0)



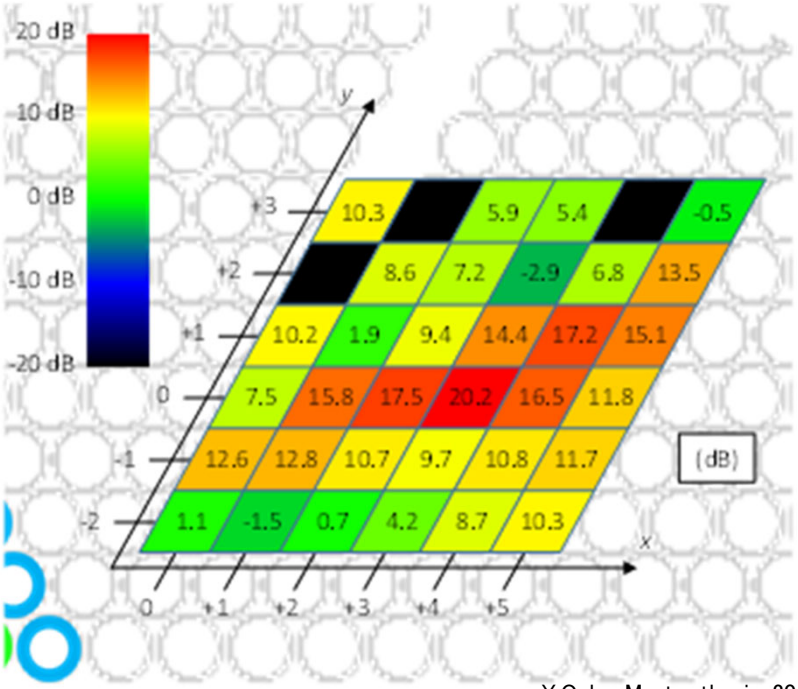
➢ Basic strategy for optimization

Suppress the undesirable peak caused by mode edge



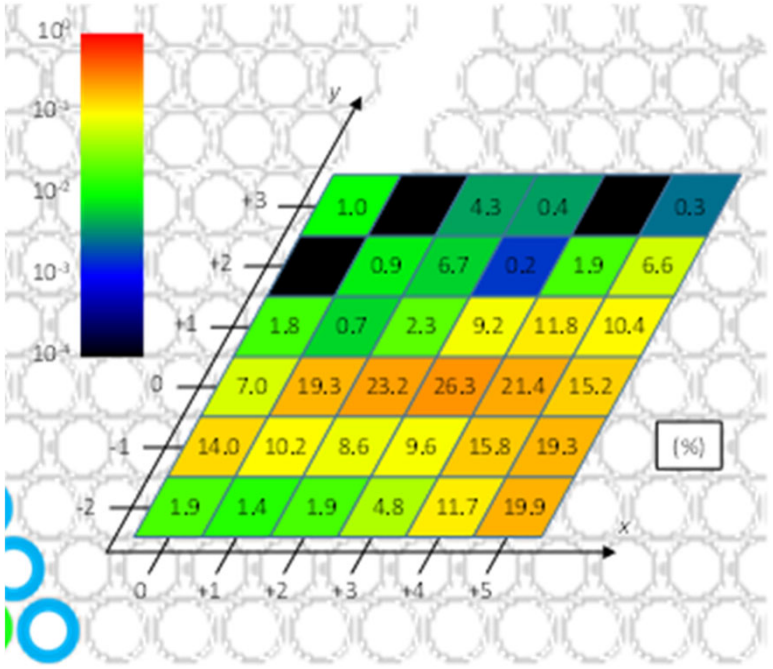
Improved crosstalk and transmittance

➢(i) Crosstalk (Simulation)



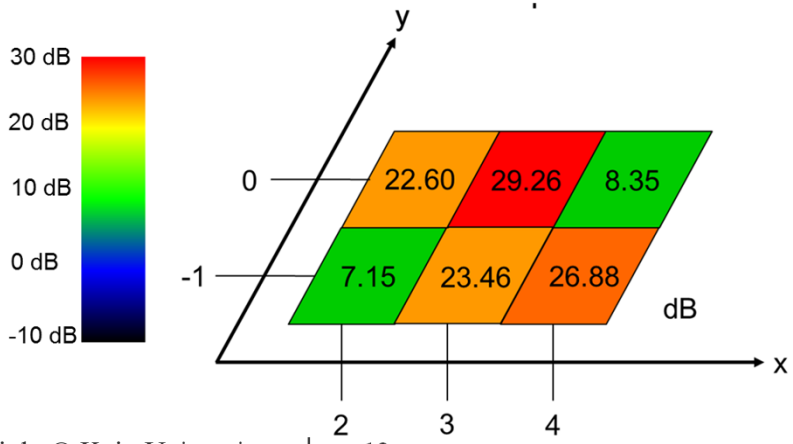
Y.Ooka, Master thesis, 2017

➢(ii) Transmittance (Simulation)

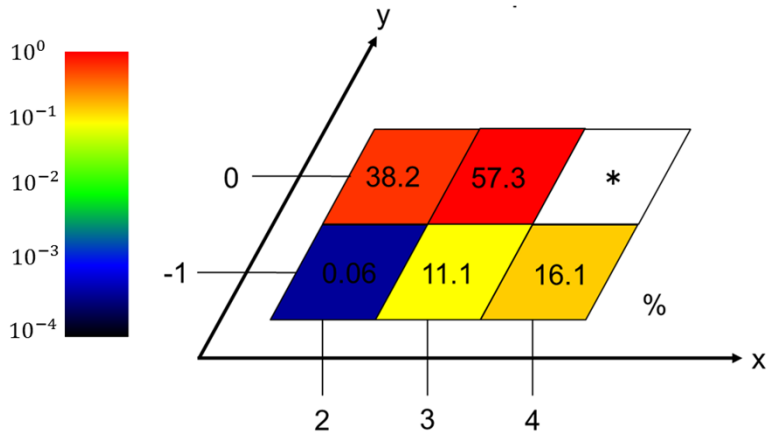


Y.Ooka, Master thesis, 2017

➢(i) Crosstalk (Experiments)

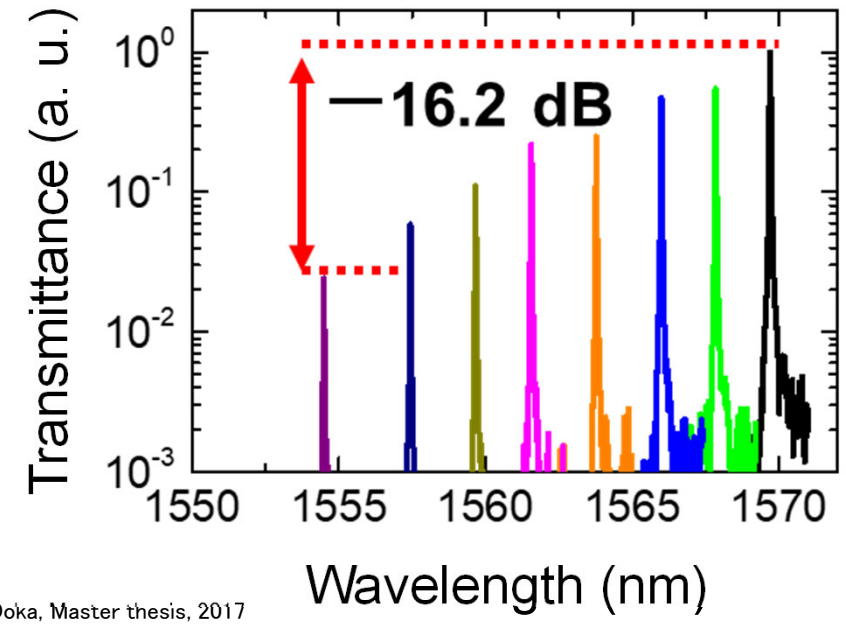


➢(ii) Transmittance (Experiments)



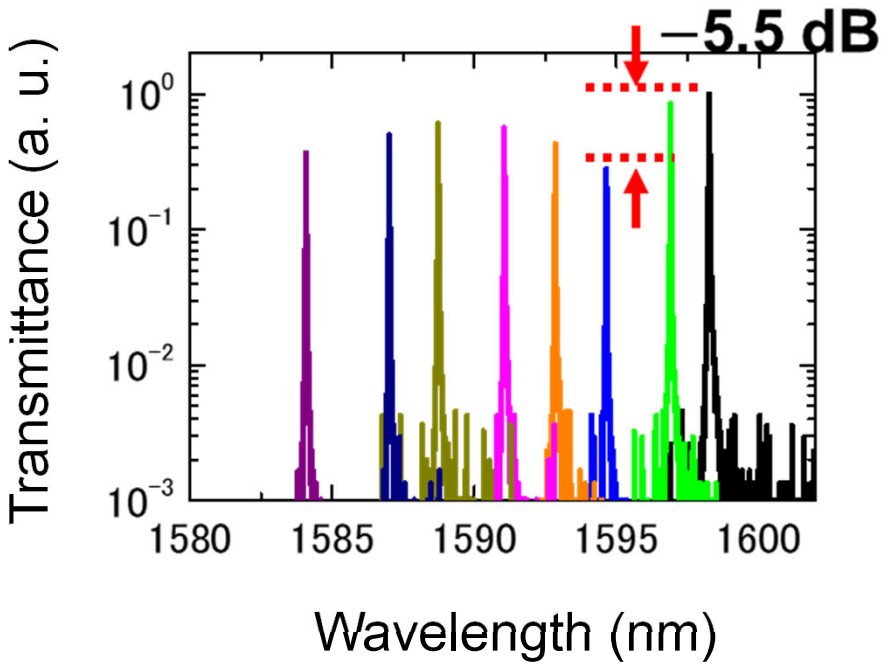
Measured spectrum

Before improvement (0,0)



Y.Ooka, Master thesis, 2017

After improvement (3,0)



	Before improvement Position : **(0,0)**	After improvement Position : **(3,0)**
Total loss (dB)	35～40	15～20
Crosstalk (dB)	−8.36	−29.3
Fluctuation (dB)	16.2	5.5

Objective (Required properties of DeMUX)

I. **Size** : 100 μm^2 order

Ultra small size is ideal in terms of on-chip integration
→PhC or plasmonic circuits

II. **Number of channel**: ～10 ch (@ ～10 Gb/s per. ch

Around 10 ch would be needed to utilize optical wi

Is it really possible to realize 100 μm^2 order？
How about influence of adjacent heaters ?

III. **Crosstalk**: －10 dB ～ －20 dB

Our target is ultra-short distance and do not need ED
Around -20 dB would be enough

IV. **Total loss**: －10 dB

Micro strip line's transmission loss: ～ - 3 dB/cm
→ Around -10 dB loss@electrical@distance: cm
Optical wiring's loss: - 0.2 dB/cm → input loss is bigger

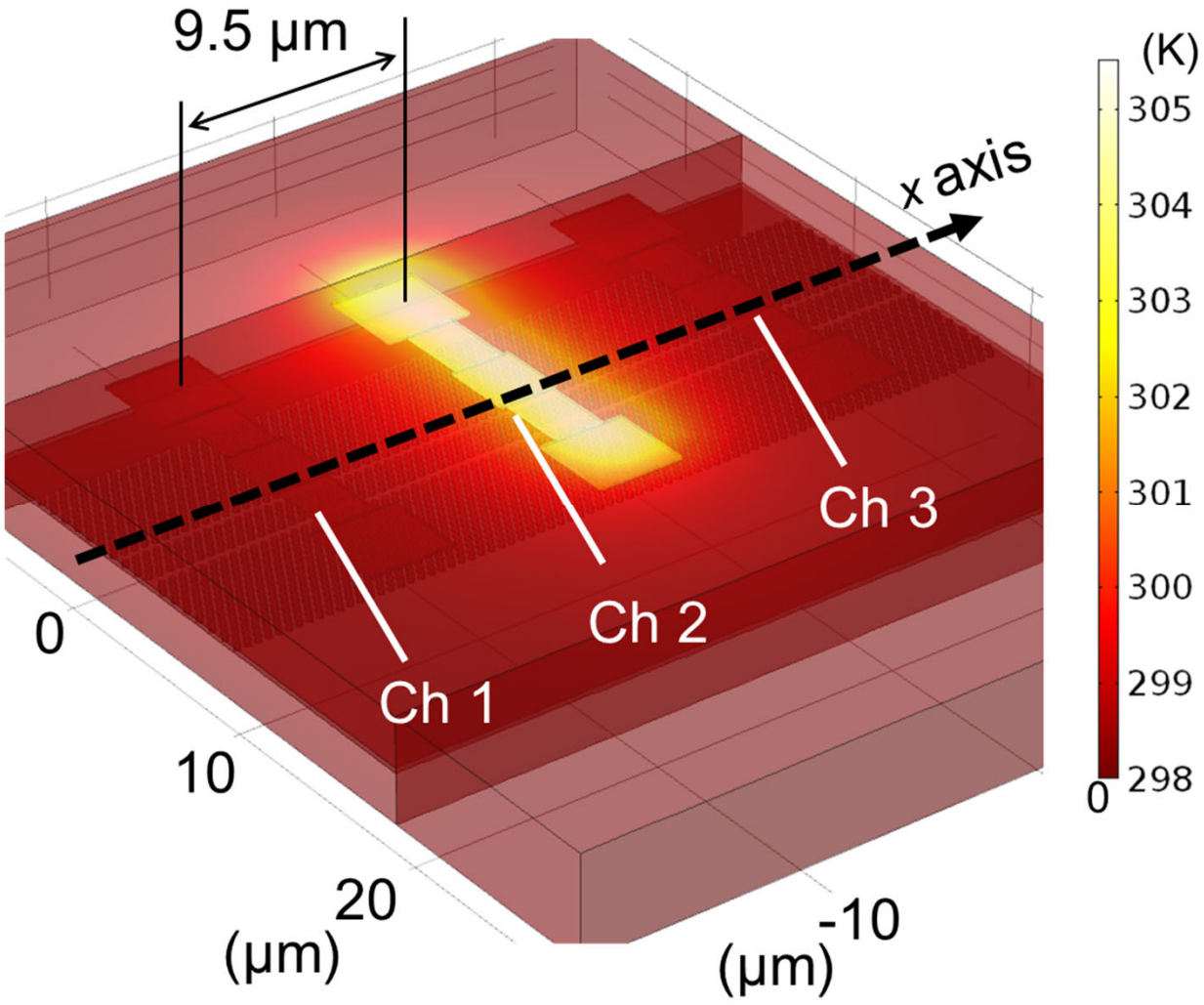
hers: Mass production(Photolithography)・Stability(SiO_2 cladding・heaters)

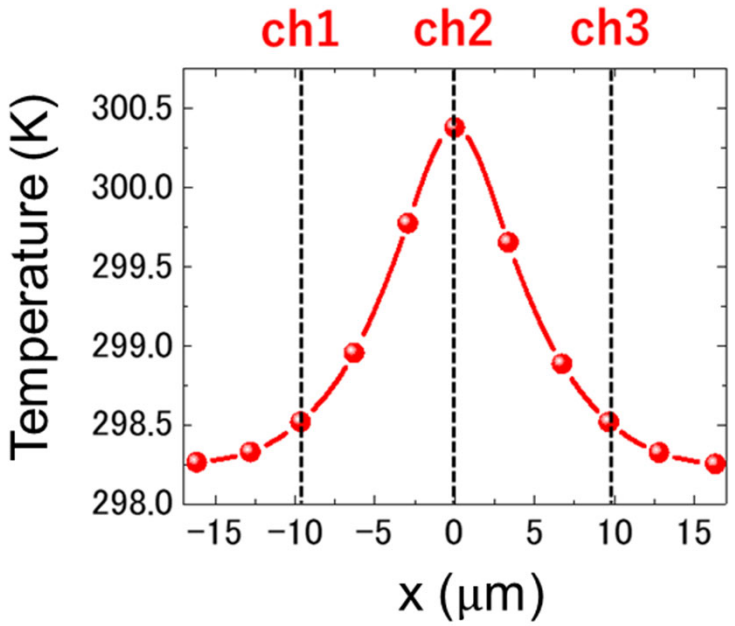
PhC DeMUX made by photolithography

Optimization of device size (heater interval)

➢Heat-flux simulation (COMSOL)

Power : 40 mW





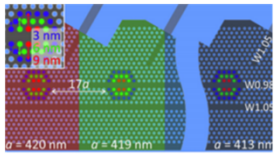
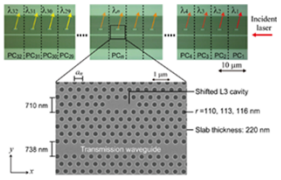
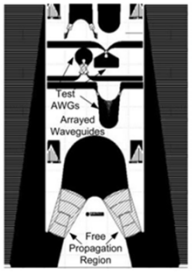
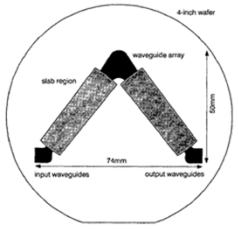
✓ Optimum heater interval

9.5 μm

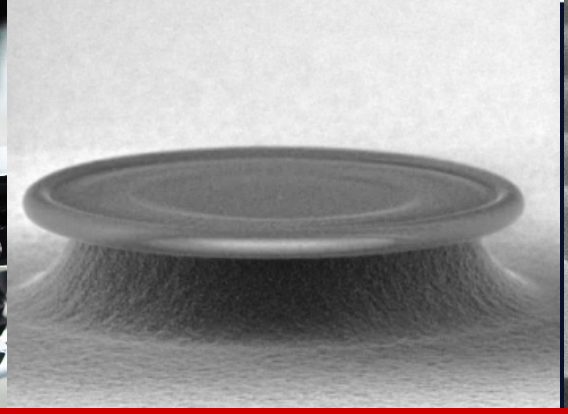
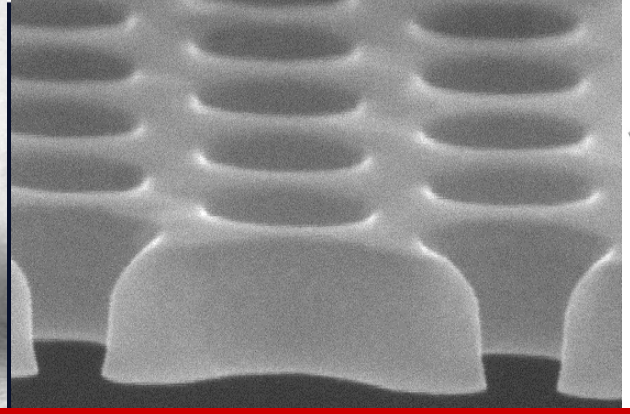
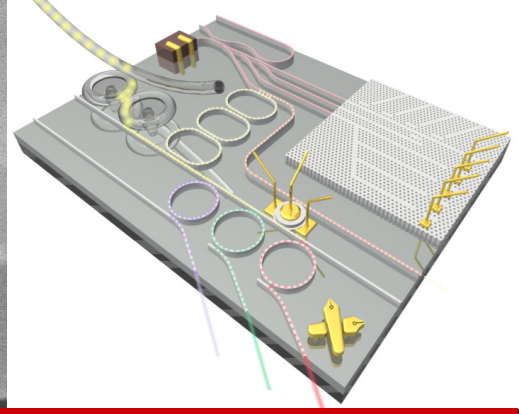
✓ Optimum size

110 μm^2/ch

Conclusion

	Our research			
		 Y. Hida, *et. al.*, OSA TOPS Vol. **54** Washington DC (2001)	 Stanley Cheung, *et.al*, IEEE, Vol. **20**, (2014)	 Y. Takahashi, *et. al.*, Opt. Exp. **22**, 4692 (2014)
Fabrication method	Photolithography	EB lithography	Photolithography	Photolithography
Number of channel	8	32	512	400
Channel spacing (GHz)	240	100	25	25
Device size (μm^2/ch)	110	100	76000	20000000
Crosstalk (dB)	−29	−	−4	−20

- We achieve crosstalk of −29.3 dB
- we could improve total loss form 35 dB to 15 dB
- We optimize the device size to 110 μm^2/ch through heat-flux simulation

Thanks for listening

Strategic Information and Communications R&D Promotion Programme (SCOPE), from the Ministry of Internal Affairs and Communications

Keio Univ